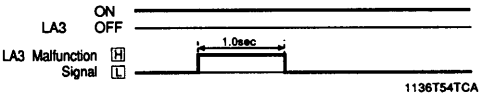
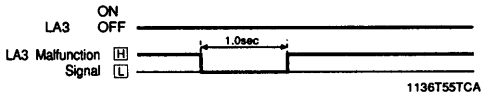
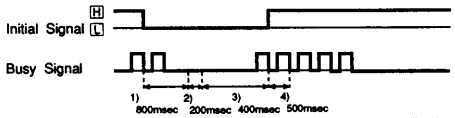
	Code	Description	Detection Timing
Erase Lamps	C0E00	Main Erase Lamp LA3's failure to turn ON	The LA3 Malfunction signal remains HIGH for a continuous 1-second period while LA3 remains ON.  1136T54TCA
	C0E01	Main Erase Lamp LA3 turning ON at abnormal timing	The LA3 Malfunction signal remains LOW for a continuous 1-second period while LA3 remains OFF.  1136T55TCA
	C0E20	Image Erase Lamp LA2's failure to turn ON	The LA2 gate array is defective according to the self-diagnoses made immediately after Main Drive Motor M1 has been deenergized.
Sensors	C0F02	Original Size Detecting Board UN2 malfunction	In F7 test operation: 1) The Busy signal does not go LOW within approx. 800 msec. after the Initial signal has gone LOW, or undefined data is input to the master CPU. 2) If 1 is checked okay, the Busy signal goes HIGH within approx. 200 msec. 3) If both 1 and 2 are checked okay, the Busy signal does not go HIGH within approx. 4,000 msec. 4) If 1, 2, and 3 are checked okay, undefined data is input to master CPU within approx. 500 msec.  1136T56TCA Under normal conditions: 1) The Busy signal remains HIGH or LOW for approx. 3,000 msec. or more. 2) Undefined data is input to master CPU.  1136T57TCA