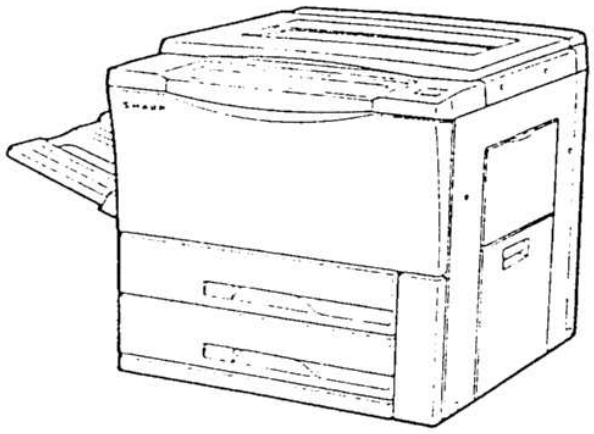
SF-2022
SF-2027

SHARP SERVICE MANUAL

CODE: 00ZSF2022TM/E



No.2

SF-2022
SF-2027
SF-D20
SF-21
MODEL SF-DM11

CONTENTS

[1] PRODUCT OUTLINE 1-1

[2] PRODUCT SPECIFICATIONS 2-1

[3] OPTIONS SPECIFICATIONS 3-1

[4] COMPONENT IDENTIFICATION 4-1

[5] PROCESS 5-1

[6] DEVELOPING UNIT 6-1

[7] PAPER FEED UNIT 7-1

[8] TRANSPORT/FUSING SECTION 8-1

[9] HIGH VOLTAGE SECTION 8-1

[10] OPTICAL SECTION 10-1

[11] ELECTRICAL SECTION 11-1

Parts marked with "⚠" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

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CONTENTS

[1] PRODUCT OUTLINE 1

1. The SF-2022 and SF-2027 are medium class copiers that produce 20 to 30 copies per minute. The SF-2022 and SF-2027 have all the standard features of medium class copiers as well as having system expansion capability similar to high end copiers. 1
2. Target users 1
3. Features 1
   (1) Compact body 1
   (2) Clean copy production without contaminating environments 1
   (3) High copy performance 1
   (4) Adoption of modular structure 1
   (5) Service, maintenance, and installation enhancement 1
4. System outline (options) 1

[2] PRODUCT SPECIFICATIONS 2

1. Basic specification 2
   (1) Type 2
   (2) Copy method 2
   (3) Kinds of originals 2
   (4) Copy speed 2
   (6) Warmup time 2
   (7) Multicopy 2
   (8) Magnification ratio 2
   (9) Exposure 2
   (10) Paper feed 2
   (11) Developing method 2
   (12) Charge method 2
   (13) Transfer method 2
   (14) Separation method 2
   (15) Fusing method 2
   (16) Cleaning method 2
   (17) Light source 2
   (18) Blanking areas 2
   (19) Automatic duplex 2
   (20) Paper eject and finishing 2
   (21) Additional features 2
   (21) Power supply 2
   (22) Power consumption 2
   (23) Appearance 2
   (24) Accessories 2
2. Consumables 2
   SF-2022/2027 consumables and option units list (SEC) 2
   SF-2022/2027 Supply Options (SECL) 2
   SF-2022/2027 Supply Options (SEEG, SUK) 2
   SF-2022.2027 Supply Options (SCA, SCNZ, Middle East, Africa) 2
   SF-2022/2027 Supply Options (Asia, Middle/South America) 2
3. Environmental requirements 2

[3] OPTIONS SPECIFICATIONS 3

1. SF-A14 3
2. SF-A54 3
3. SF-S14 3
4. SF-S15 3
5. SF-S52 3

6. SF-D20 ... 3-2
7. SF-D21 ... 3-2

[4] COMPONENT IDENTIFICATION ... 4-1
1. External view ... 4-1
2. Operation panel ... 4-3
3. Internal view ... 4-5
4. Clutches, solenoids ... 4-6
5. SF-2022 2027 sensors ... 4-7
6. Motors ... 4-8
7. Board list ... 4-9
8. Duplex copy tray ... 4-10
9. Desk unit (SF-D20) ... 4-11
10. Desk unit (SF-D21) ... 4-12

[5] PROCESS (Photocondor drum and cleaning unit) ... 5-1
1. Basic theory ... 5-1
(1) Image forming process ... 5-1
(2) Photoconductor ... 5-1
(3) Types of photoconductors ... 5-1
(4) Characteristics of photoconductor ... 5-2
2. SF-2022/2027 basic process and structure ... 5-3
(1) Details of image forming process ... 5-3
(2) Relationship between the OPC drum and light ... 5-4
(3) Transition of photoconductor surface potential ... 5-5
(4) Photoconductor drum sensitivity correction ... 5-5
3. Basic structure ... 5-5

[6] DEVELOPING UNIT ... 6-1
1. Basic theory ... 6-1
(1) Two-component developer ... 6-1
(2) Two-component magnetic brush development ... 6-1
(3) Developing bias voltage ... 6-1
2. Structure ... 6-1
3. Operation ... 6-1

[7] PAPER FEED UNIT ... 7-1
1. Outline ... 7-1
2. Basic configuration ... 7-1
3. Basic operation ... 7-2
(1) Manual paper feed operation ... 7-2
(2) Cassette paper feed operation ... 7-3

[8] TRANSPORT/FUSING SECTION ... 8-1
1. General ... 8-1
2. Basic composition and functions ... 8-1
(1) Transport section ... 8-1
(2) Fusing section ... 8-1

[9] HIGH VOLTAGE SECTION ... 8-1
1. General ... 8-1
2. Basic composition ... 8-1
(1) Main (charging) corona – High voltage transformer (MHVG) ... 8-1
(2) Transfer corona – High voltage transformer (THVG) ... 8-1
(3) Separation corona – High voltage transformer (SHVG) ... 8-1

[10] OPTICAL SECTION 10-
1. General .....
2. Basic composition 10-
(1) Original table 10-
(2) Copy lamp 10-
(3) Mirror 10-
(4) Lens (Fixed focus lens) 10-
(5) Lens home position sensor (LHPS) 10-
(6) No. 4, No. 5 mirror base home position sensor (MBHPS) 10-
(7) Lens base 10-
(8) Lens slide shaft 10-
(9) Lens drive wire 10-
(10) Mirror base C 10-
(11) Mirror base C (No. 4, No. 5 mirrors) drive wire 10-
(12) Mirror motor 10-
(13) Mirror home position sensor (MHPS) 10
(14) Mirror base B 10
(15) Copy lamp unit 10
(16) Thermal fuse 10-
(17) Reflector .....
(18) Exposure adjusting plate 10
(19) Mirror base drive wire 10
(20) Mirror base (No. 4, No. 5) drive motor 10
(21) Lens drive motor 10
(22) AE sensor 10
(23) Blank lamp operation 10
(24) Original size detection 10
3. Basic operation 10
4. Optical system dirt correction 10
(1) Setting the reference value for optical system correction. 10
(2) Dirt correction 10-

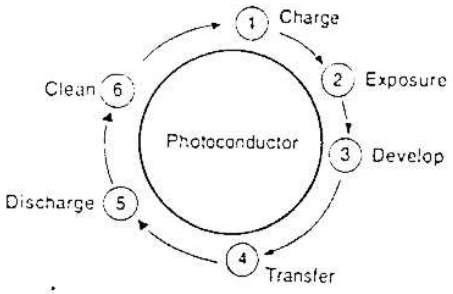
[11] ELECTRICAL SECTION 11
1. System Block Diagram 11
2. Main circuit 11
(1) Block diagram 11
(2) CPU (IC113) H8/570 .....
(3) I/O (IC114) TE7750 11
(4) RAM (IC115) X28C64 11-
(5) Decoder (IC139, IC138) 11-
(6) Start/stop control circuit 11-
(7) Heater lamp control circuit 11-
(8) Driver circuit (Solenoid, magnetic clutch) 11-
(9) Stepping motor drive circuit 11-
(10) AE (Auto Exposure) sensor circuit 11-
(11) Toner supply motor drive circuit 11-
3. Operation circuit 11-
4. Desk circuit 11-
(1) Block diagram 11-
(2) Circuit block diagram 11-
(3) Cassette size detecting section 11-
(4) 24V monitor and door open detecting section 11-
(5) Output section 11-
(6) Overcurrent detecting section .....

[5] Process (Photocondor drum and cleaning unit)

1. Basic theory

With the indirect static copier, a plain paper is used for the copy paper. As a latent static image is formed on the surface of the photoconductor, the image is then developed into visible (toned) image using the toner. Then the toner is transferred onto the copy paper.
The plain paper copier (PPC) has six basic processing steps of corona charge, exposure, development, transfer, discharge, and cleaning. The cleaning step prepares the photoconductor surface for repeated use.

(1) Image forming process



① Corona charges the photoconductor.

② The photoconductor is exposed to light to form a static latent image.

③ Toner is attracted to the static latent image.

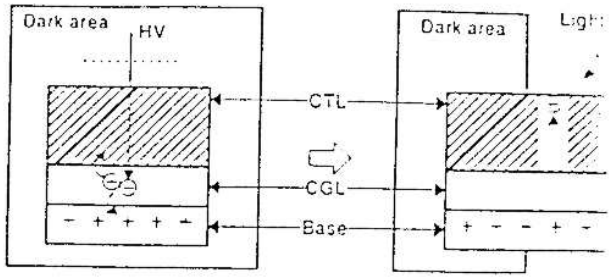
④ The toner on the drum is transferred onto the copy paper.

⑤ The charge remaining on the photoconductor surface (residual charge) is removed.

⑥ Toner remaining on the photoconductor (residual toner) is removed.

(2) Photoconductor

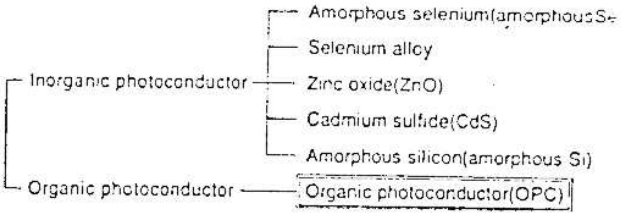
While some materials conduct electricity, others do not. Materials, therefore, can be put into three categories of conductor, semiconductor, and insulator.
For these categories are conceptual, distinct classification is difficult. Generally, the following is applied.
Material whose specific resistance is over $10^3\Omega$cm is called insulator and under $10^{-3}\Omega$cm is called conductor.
Those which existing between the two is normally called semiconductor.
Conductor in the category always has the electrical conductivity, while semiconductor does not. But, it may become conductor under certain conditions.
The photoconductor used by the copier is an insulator when not exposed to light, but its electrical resistance abates when exposed to light. When exposed to light, the photoconductor surface becomes conductive. Material having the property to become conductive in light (photo conductive phenomenon) is a photoconductor or photosemiconductor.



Theory of photoconduction

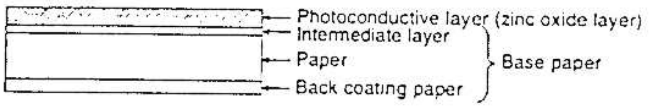
(3) Types of photoconductors

The pricipal materials of a photoconductor are zinc oxide (ZnO), amorphous selenium (amorphous Se), selenium alloy, cadmium sulfide (CdS), amorphous silicon (amorphous Si), and organic photoconductor (OPC).

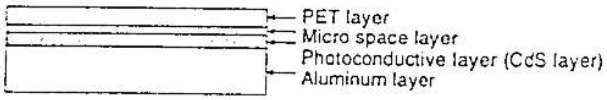


Described next are structures of the photoconductors we have used up to now.

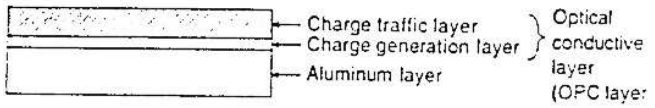
Zinc oxide (ZnO) master



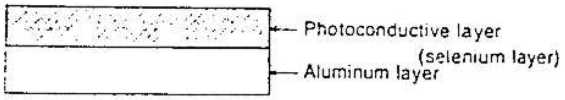
Cadmium sulfide (CdS) drum



Organic photoconductor (OPC) master and drum



Selenium (Se) drum



	ZnO	OPC	CdS	Se
Photoconductivity	4	3	2	1
Photoconductor strength	4	3	2	1
Photoconductor life	Several hundred cycles	Several ten thousand cycles	Several ten thousand cycles	Several hundred thousand cycles

Photoconductor characteristics
1 > 2 > 3 > 4

Characteristics of organic photoconductors

- Permits a variety of structures (drum, sheet, belt)
- Higher insulation in dark area (charge acceptability and retentivity)
- Permits a variety of molecular structure (allows a variety of molecular design)
- Light weight
- Stable against humidity and temperature
- Safety for environment (non-pollution, unrestrained disposal)
- Not strong in anti-wear property
- Not strong against light and ozone.

haracteristics of photoconductor

Mentioned next is the general characteristics important to use for the photoconductive material.

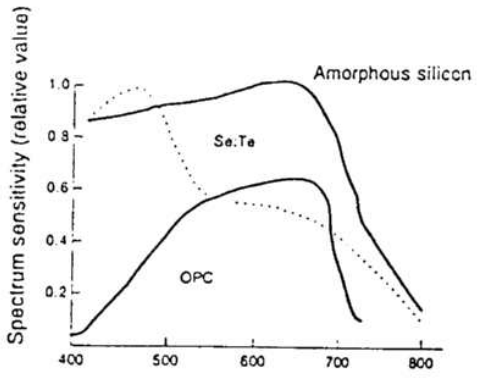
1. Photo-sensitivity
2. Spectrum characteristics
3. Acceptor potential
4. Charge retentivity
5. Residual potential
6. Fatigue

[Photo-sensitivity]

This is dependent on the attenuation speed of the potential when the photoconductor is exposed to light.

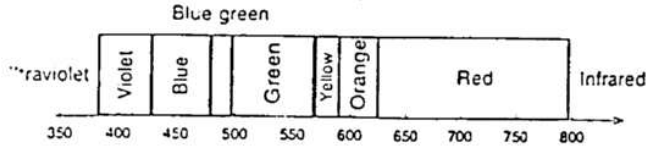
[Spectrum characteristics]

Wave length of the light differs by the kind of the photoconductor.



Spectrum sensitivity

Relationship between color and wave length
Light having wave length of 380mm through 780mm can be recognized by human eyes, which is called visible light. Wave length shorter than that is called ultraviolet light and the longer than that is called infrared light. Figure below shows the relationship between the wave length of light and color.



[Acceptor potential]

The resistance in the dark area of the photoconductor decreased as the electric field increases among layers.
As the electric field is formed to a higher value as the photoconductor is charged, the resistance in the related layer decreases and the rate of charge retained in the photoconductor is restricted. The potential of the photoconductor in this instance is called acceptor potential which is the important factor to determine the potential contrast. To avoid giving electrical distortion in the photoconductor, charge is normally made to a level slightly lower than the acceptor potential.

[Charge retentivity]

The time the static latent image is held by the photoconductor depends on the speed at which the potential decreases in the dark area. For this, measure the time the photoconductor potential abates to a half of the starting value in the dark area. This charge retentivity may cause a problem when the time from the exposure to the development is long. But, it may not be a problem with the machine where a series of operations from charge, exposure, and development are automated and time between processes is shorter.

[Residual potential]

When the charged photoconductor is exposed to light, the potential abruptly diminishes at first, then begin decaying relatively slowly. The potential of the photoconductor where slow decay starts is called residual potential. For a less residual potential produces a large potential contrast, low residual charge is preferable.
The value of the residual potential affects largely to the development of gradual tone.

[Fatigue]

If charge and exposure are repeated, the phenomenon called photoconductor fatigue occurs. In other words, it appears as an increase of the decay speed of the photoconductor potential or a decrease in the charge retentivity.

Now, we have learned about the characteristics required for charging of the photoconductor. If charge is repeated from the corona unit in the actual operation, the corona wire is likely to be contaminated with dust, stain, and scattered toner, causing uneven corona charge. To avoid this, the corona wire needs to be cleaned well.

2. SF-2022/2027 basic process and structure

- The Scorotron method is used to evenly charge the photoconductor surface to the given potential in the charge process. The corona wire regularly used is now replaced with a new corona charge mechanism that employs the 0.1mm thick stainless steel saw teeth plate, in order to suppress ozone generated when the oxide molecule in air is ionized.
- Considering the service efficiency, the process separation mechanism is adopted.
- To prevent high voltage leakage by the loose corona charge unit, a one-touch stopper mechanism is adopted.



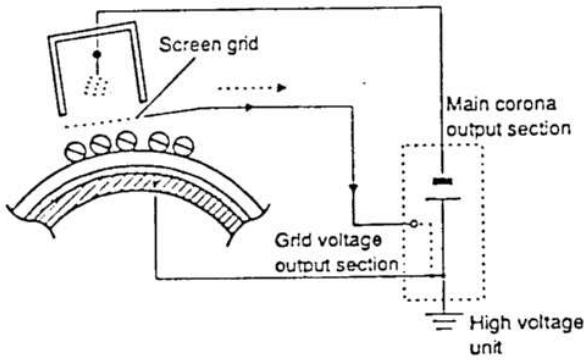
Drive system diagram

(1) Details of image forming process

STEP 1. Charging (DC-700μA)

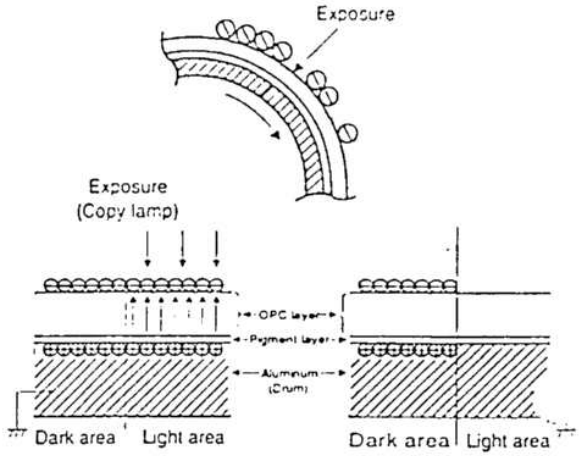
(grid voltage refer page 8-1)
The main corona discharges negative corona to give negative charges to the OPC drum surface evenly.
The surface potential of the OPC drum is controlled by the screen grid voltage to maintain at the potential equal to the grid voltage.

- When the drum surface voltage is lower than the screen grid voltage, electric charges from the main corona pass through the screen grid to reach the drum surface and charge it until the drum surface voltage becomes equal to the grid voltage.
- When the drum surface voltage reaches almost the same level as the grid voltage, electric charges from the main corona flow through the electrode of the screen grid to the high voltage unit grid voltage output circuit, thus maintaining the drum surface voltage at the same level as the grid voltage.



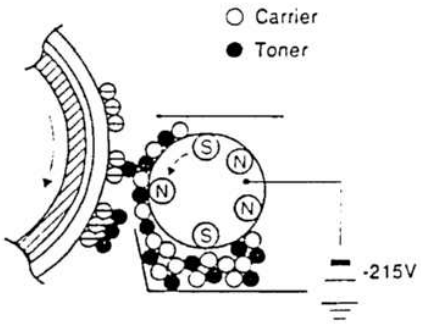
STEP 2. Exposure (Copy lamp, mirror, lens)

The optical image of an original is projected through the m ir lenses onto the OPC drum surface by the copy lamp. The re. .nc of the OPC layer reduces in the bright area (light area on the origin to discharge negative charge, forming an electrostatic latent image the drum surface.
In reduction copy, the non-image area of the image is discharged the BL (blank lamp) before exposure.



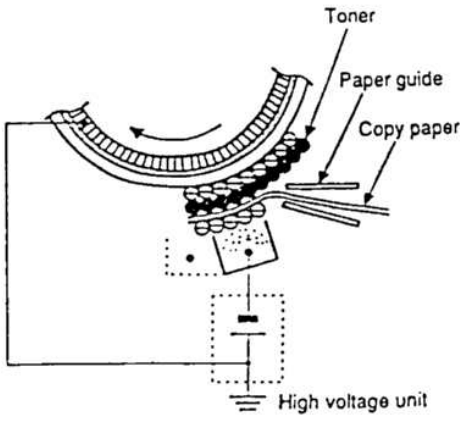
STEP 3. Development (Bias –215V)

The electrostatic latent image on the drum surface is formed into visible image by the toner. This copier employs the two-componer magnetic brush development system, where a bias voltage of –215 is applied to the carrier (MG roller) and the toner is charged positivel by friction with the rotating carrier.



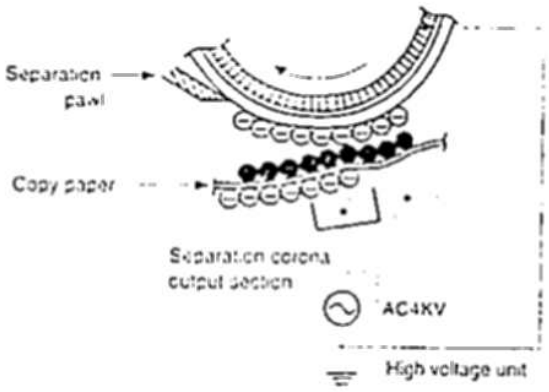
STEP 4. Transfer (DC –31μA)

The visible image on the drum surface is transferred on to the cop paper. A negative charge of the transfer corona is applied to the rea surface of the copy paper to transfer the toner on the drum surface t the copy paper.



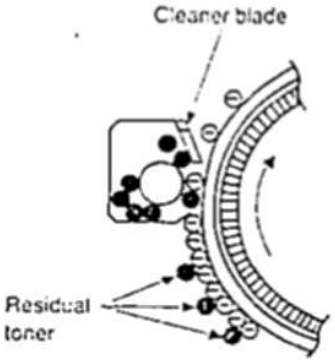
STEP 5. Separation (AC4KV)

Though the copy paper and the drum are both negatively charged by transfer, the negative potential on the drum is higher than that on the copy paper, generating an attraction force between the drum and the copy paper. To remove the attraction force, AC corona is applied to the copy paper by the separation corona to raise the potential on the copy paper to the same level as the drum surface potential. Resultantly the attraction force is eliminated and the copy paper is separated from the drum. If the paper is not separated from the drum, the separation pawl works to separate it mechanically.



STEP 6. Cleaning

Residual toner on the drum is collected by the cleaning blade.



STEP 7. Discharge

The electric resistance of the OPC layer is reduced by radiation from the discharge lamp over the drum to remove residual charges.

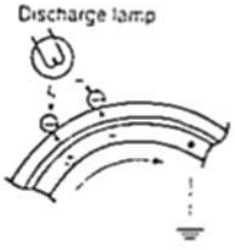
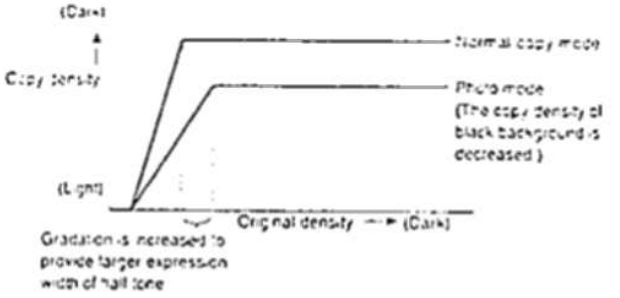


Photo mode

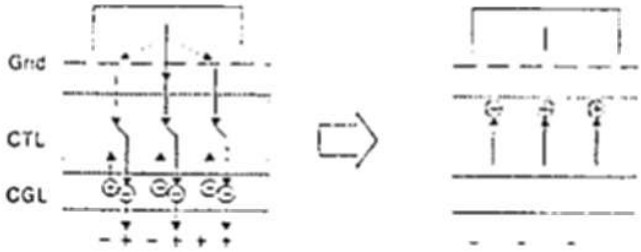
The photo mode is provided to make clear half-tone copy of the photo originals.

In the photo mode, the grid voltage and the copy lamp voltage are lowered than in the standard copy mode (the copy density of the black background is lowered) to provide half tone gradations of the copy.

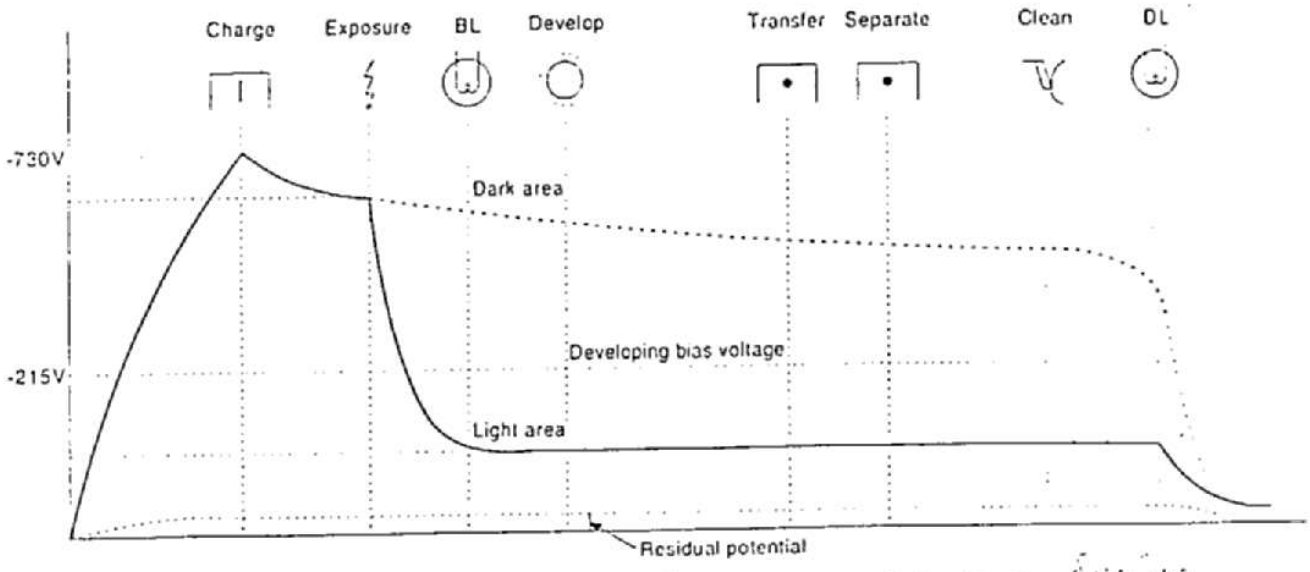


(2) Relationship between the OPC drum and light

The light exposed is absorbed by the charge carrier generation layer (CGL) to generate the charge carrier and moves towards the charge carrier transport layer (CLT). The carrier reached CTL then moves towards the drum surface through CTL to neutralize the surface charge.

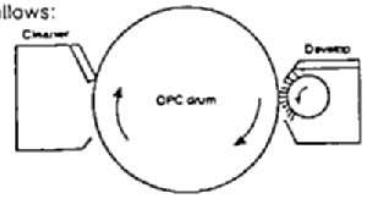


(3) Transition of photoconductor surface potential



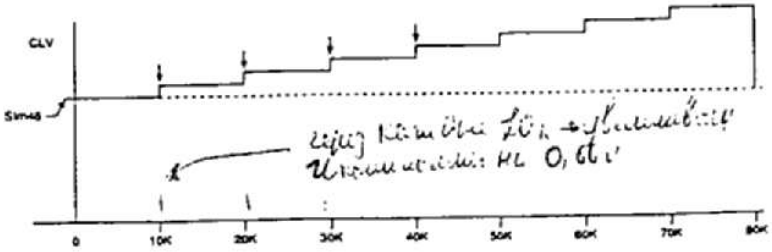
(4) Photoconductor drum sensitivity correction

In the SF-2022/2027, fall in sensitivity due to long use of the photoconductor drum is corrected by the copy lamp light intensity to prevent against considerable change in copy quality.
The photoconductor drum sensitivity fall correction is performed as follows:



Change the tickness of the carrier transport layer (CTL).
By the developper.
By the cleaner blade.





CLV + 2 counts ⟹ CL(V) + (0.33V x 2)
(Sim46)

3. Basic structure

Photoconductor drum:	The 65mmø ground plate of the OPC drum is on the rear frame side of the drum unit so that it contacts the drum locator pin.
Blank lamp:	The non-image area is exposed by the light from the blank lamp to erase the positive potential outside the drum CTL. Use of the latchet simplifies the lamp position adjustment.
Discharge lamp:	Eight bulbs cast light over the drum surface to erase the positive potential in CTL. Ventilation hole provided in the drum frame releases heat from bulbs.
Cleaning mechanism:	The cleaning blade removes the toner remaining on the drum surface. The blade always rests on the drum surface.
Main corona:	The saw teeth corona charge method is used. Use of the screen grid maintains the even charge potential over the photoconductor surface.
Enforced separation mechanism:	Using two pieces of separation pawl, the copy paper stuck over the drum surface is forced to separate from the drum surface
Waste toner transport mechanism:	To enhance the toner transport efficiency the transport pipe is used and toner clog up is avoided by setting the waste toner transport path downward.

[6] DEVELOPING UNIT

1. Basic theory

(1) Two-component developer

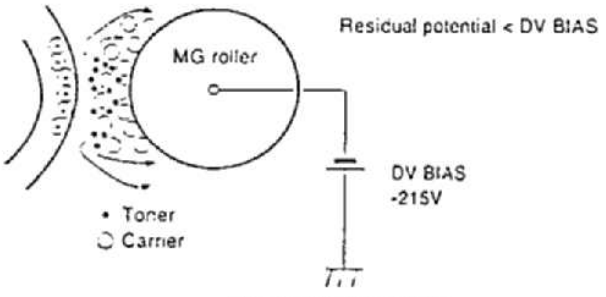
The developer consists of toner and carrier, which is usually called developer.
The carrier is a media that applies toner to the static latent image on the photoconductor.
As the carrier is stirred with the toner, the friction occurred thereby charges it to positive or negative.
Because the developer fatigues and affects its characteristics that deteriorates the copy quality, it needs to be replaced with a fresh one at a given period.

(2) Two-component magnetic brush development

A rotary, non-magnetic sleeve is provided over the magnet roller and is rotated.
Carriers forms the magnetic brush on the sleeve surface by magnetic force to make toner be attracted onto the latent electrostatic image on photoconductor.

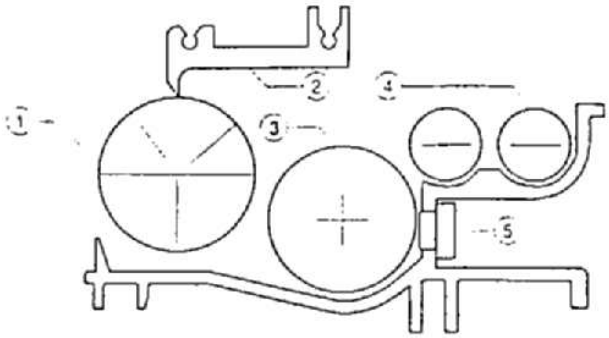
(3) Developing bias voltage

When the photoconductor is exposed to light, the surface potential (voltage) of the photoconductor is not removed completely and remains as a residual potential. Therefore, the toner stuck on the photoconductor by the residual potential stains a white area of the copy background.
To prevent this, a voltage of the same charge on the photoconductor surface which is higher than the charged potential is added to the magnetic roller to avoid the toner from remaining on the photoconductor surface.



Developing bias voltage

2. Structure



No.	Name	
1	Developer mangetic roller	Magnetic brush is formed to the carrier by the magnetic force.
2	Developer doctor plate	A plate employed to limit the height of the magnetic brush.
3	Developer stirring roller	Carrier within the developing unit is stirred to distribute the toner evenly.
4	Developer transport roller	The toner fed from the toner hopper is supplied to the stirring unit.
5	Toner density sensor	Used to detect the density of the toner contained in the developer.

3. Operation

When the power is turned on, the machine goes into the warmup mode and the main motor starts to run in 1.5 minutes.
The developer unit is driven by the main motor via the main drive unit.
Ratio of the carrier and the toner within the developing unit is monitored by the toner density sensor as a change in the magnetic transmission rate and the voltage is sent to the analog input line of the CPU of the main board.
In the CPU, the input voltage level is monitored and the main motor and the toner motor is controlled until the optimum density is obtained. Then the toner is supplied, transported, and stirred.

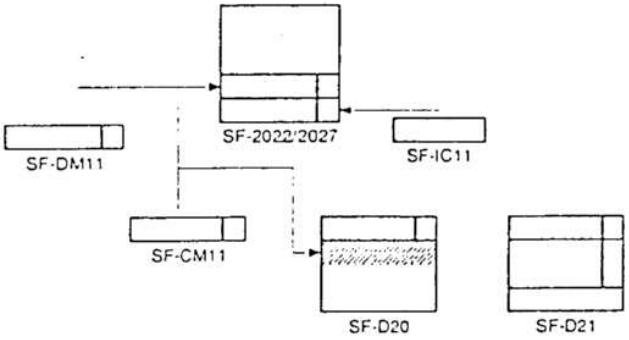

Drive system diagram

[7] PAPER FEED UNIT

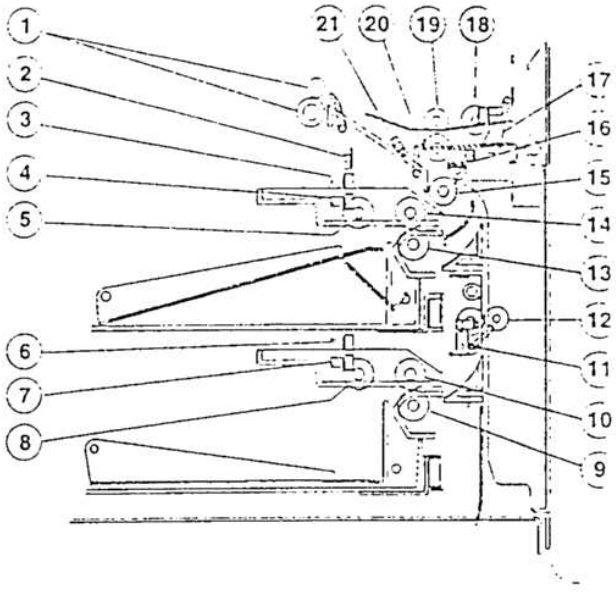
1. Outline

The front load method and the foldable multicopy table are provided to save space. The machine is equipped with two 500-sheet cassettes and a manual feed multicopy table that may feed up to 50 sheets. Use of a desk unit option and a cassette module allows to expand the system.

Standard setting



2. Basic configuration

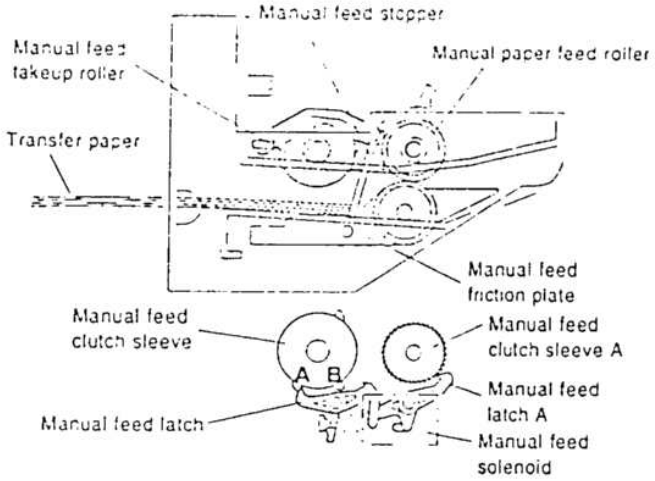


No.	Name	
1	Resist roller	Synchronizes the copy paper with image by controlling the resist roller clutch (RRC).
2	(PPD2) Paper transport sensor	For control of the paper transport roller clutch (TRC).
3	(LUD2) Lift upper limit sensor	For control of the upper cassette liftup motor; a high on this line stops the motor.
4	(PED2) Paper presence sensor	For detection of paper in the upper cassette; a low on this line shows that paper is present.
5	Takeup roller	The upper cassette paper takeup roller descends at the moment the paper feed solenoid turns on.
6	(LUD3) Lift upper limit sensor	For control of the lower cassette liftup motor; a high on this line stops the motor.
7	(PED3) Paper presence sensor	For detection of paper in the lower cassette; a low on this line shows that paper is present.
8	Takeup roller	The lower cassette paper takeup roller descends at the moment the paper feed solenoid turns on.
9	Counter paper feed roller	For prevention of double feed paper using the lower paper reversion roller.
10	Paper feed roller	Lower cassette paper feed roller with an internal one-way clutch.
11	(PID) Paper entry sensor	Entry of paper from the lower cassette is sensed to turn off the paper feed solenoid.
12	Paper transport roller	For transport of paper from the lower paper cassette.
13	Paper reversion roller	For prevention of double feed paper using the upper paper reversion roller.
14	Paper feed roller	Upper cassette paper feed roller with an internal one-way clutch.
15	Paper transport roller	Paper from the cassette is transported to the resist roller.
16	(TFD) Full waste toner sensor	A low on this line shows the full toner condition.
17	(PED1) Paper presence sensor	For detection of manual feed paper; a low on this line shows the paper is present.
18	Takeup roller	Manual feed paper takeup roller
19	Paper feed roller	Manual paper feed roller with one-way clutch
20	Paper reversion roller	For prevention of double feed paper using the lower paper reversion roller.
21	(PPD1) Paper transport sensor	For detection of paper from cassette and manual paper feed.

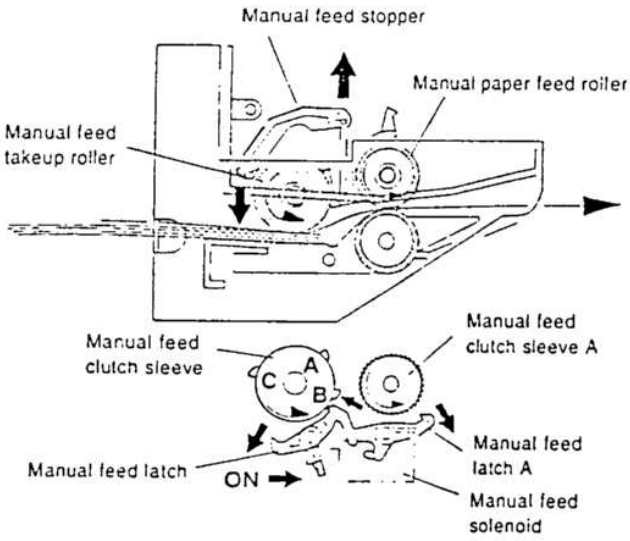
3. Basic operation

Manual paper feed operation

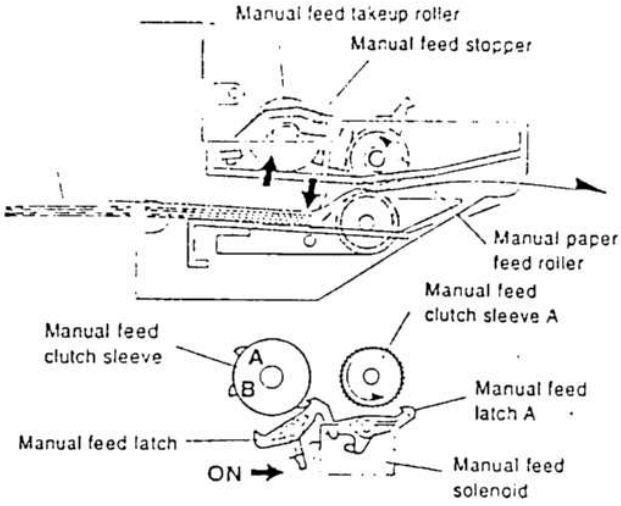
1 When the manual feed is at rest, the manual paper feed solenoid (MPFS) is off and the manual feed stopper is closed with the takeup roller in the up position. Latches and clutches are in the position shown in the figure below.



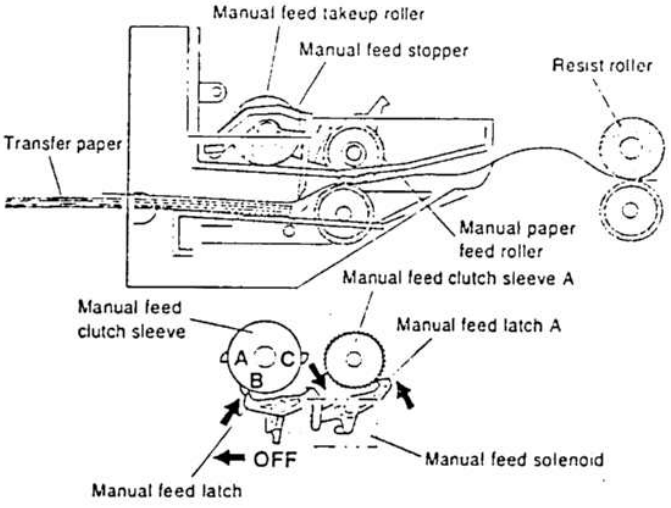
2 When the PRINT switch is pressed, the manual paper feed solenoid (MPFS) turns active, the manual feed latch A disengages from the manual feed clutch sleeve A, and the manual feed roller and the manual feed takeup roller start rotating. In this moment, the manual feed stopper opens and the manual feed takeup roller comes in close contact with the copy paper to start paper feed.



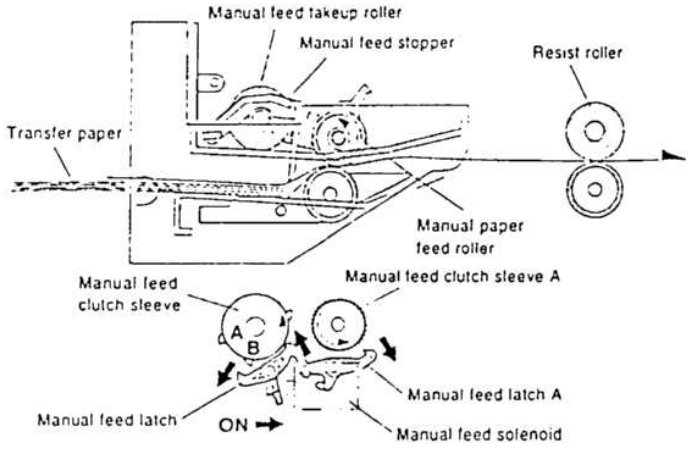
3 When the pawl C of the manual feed clutch sleeve B7 is caught by the manual feed latch B7, the manual feed stopper goes down and the manual feed takeup roller goes up. At this moment, the transport roller is rotating.



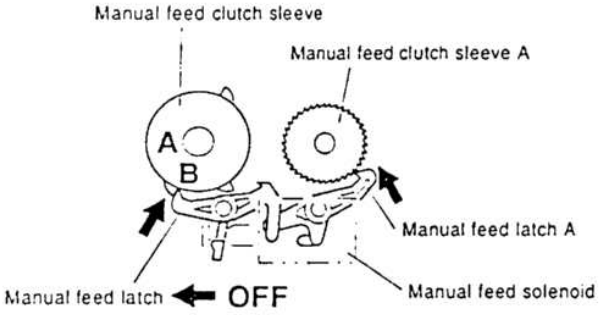
④ After the lead edge of the copy paper is detected by PPD2, the manual feed solenoid turns off after 0.2 second. Here, the pawl B of the clutch sleeve B7 is caught by the manual feed latch B7. This produces a buckle in the paper between the resist roller and the paper feed roller.

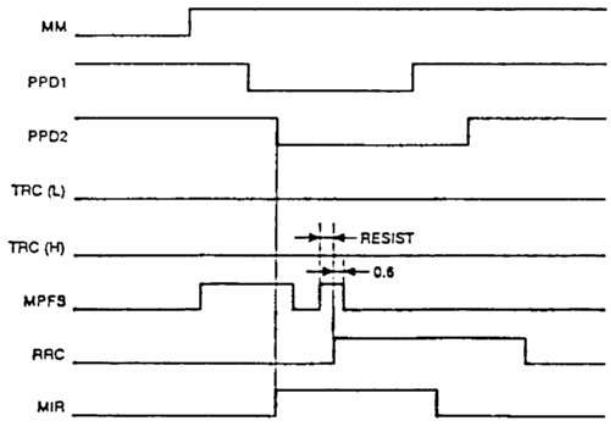


5 In synchronization with rotation of the resist roller, the manual feed solenoid turns on for 0.08 seconds and the manual paper feed roller rotates. A misfeed caused by a lack of seizure of the resist roller is prevented. Here, the manual takeup roller is up.



6 The manual feed solenoid turns off, the pawl A of the manual feed clutch sleeve B7 is caught by the manual feed latch B7, the manual feed operation terminates. The copy paper is then sent to the transfer unit by way of the resist roller.





(2) Cassette paper feed operation

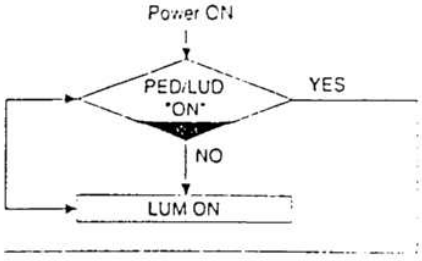
For the upper, lower, and desk cassettes, paper is fed in the same manner.

The operations of the lower cassette are described below.

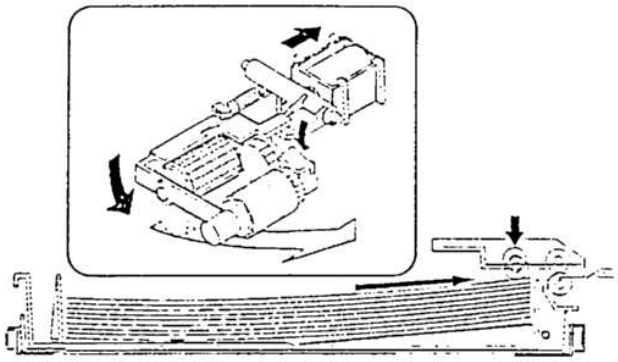
1 Liftup action

When the power is turned on to the copier, the main [illegible] itiates to check every sensor.

The liftup motor is turn on or off according to the state of th paper presence sensor (PED) and the liftup sensor, and it be comes ready to feed paper.



→ CPFS2 turns on and the take-up roller presses the copy paper to start paper feed.



2 Paper feed operation

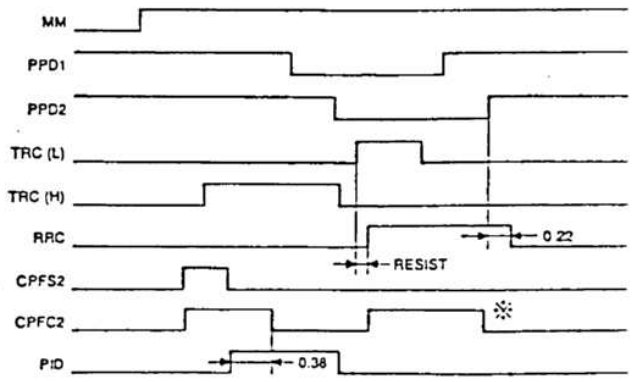
When the PRINT switch is pressed, the cassette paper fee solenoid (CPFS2) and the cassette paper feed clutch (CPFC2 turn on. As the solenoid turns on, the paper takeup roller is force down to make contact with paper.

As the clutch turns on, the paper feed roller and the takeup roll start to rotate to pick up paper.

The paper picked up passes over the paper entry sensor (PI and sent to the paper transport roller area.

The paper transport roller is driven with two kinds of clutches Paper transport from the paper feed block to the resist roller performed with the high speed clutch.

The paper obstructed by the resist roller synchronizes [illegible] th optical unit and transported to the process unit. For the paper transported at the same speed as the process unit rotation, th drive changes from the high speed clutch to the low speed clutch



Lower cassette paper feed timing chart

÷ 500 ms ON when A3 (11"x17") paper feeding with the lower cassette.

[8] TRANSPORT/FUSING SECTION

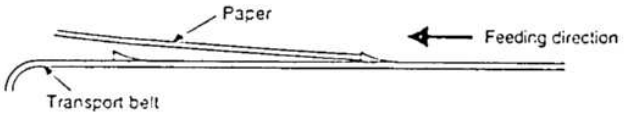
1. General

The SF-2022/2027 allows transport of paper of max. A3 (11" x 17") and min. A5 (8 1/2" x 5 1/2").
After images are transferred on the paper, the paper is separated from the drum and transported to the fuser section by rotations of the resist roller and the transport belt.
The paper separation sensor (PSD) is provided at the transport section. This sensor (PSD) is used to sense paper separation and for drive timing of the duplex gate solenoid (DGS) after fusing.

2. Basic composition and functions

(1) Transport section

1 Transport belts (2pcs)
The transport belts are provided with notches to hold paper rear ends.



2 Separation sensor (PSD)
This is a transmission type sensor, and attached to the main body chassis.

3 Suction fan motor and ozone filer
Ozone generated in the process high voltage section is absorbed through the filter.

(2) Fusing section

① Upper heat roller
The upper heat roller is teflon-coated. (Reversed crown shape)

② Lower heat roller
A silicone rubber roller is used. (Crown shape)

③ Upper cleaning roller
The upper cleaning roller is impregnated with silicone oil to remove dirt on it and to provide better separation effect, lengthening the heat roller lifetime.

④ Separation pawl
The upper heat roller is equipped with four pawls which are teflon coated to reduce friction.
the lower heat roller is equipped with two pawls.

5 Upper/lower separation function
The upper and lower heat roller sections are separated by rotating operations with the transport roller as a fulcrum, providing better serviceability.

6 Drive system division
The fuser unit is rotated by the main drive unit. In case of manual rotation of the fuser unit to remove paper jam, however, excessive loads may be applied to the gears. To prevent against this, the spring clutch is provided in the main drive gears.



[9] HIGH VOLTAGE SECTION

1. General

There are three kinds of coronas: the main corona, the transfer corona, and the separation corona. The main corona employs the scorotron system, where the drum surface is evenly charged with negative charges controlled by the screen grid between the corona and the drum. The transfer corona is used to transfer toner images on the drum to the copy paper. A high, negative voltage is applied to the rear side of the paper. The separation corona applies AC corona to the copy paper to eliminate potential difference with the drum to allow separation of the paper.

2. Basic composition

(1) Main (charging) corona – High voltage transformer (MHVG)

–700µA (Electrode sheet front-rear balance difference: max. 8µA)

	Grid voltage	Developing bias voltage
Standard mode	–730V	–215V
Photo mode	–450V	
TSM mode	–610V	

(2) Transfer corona – High voltage transformer (THVG)

–31µA (Electrode sheet front-rear balance difference: max. 8µA)

(3) Separation corona – High voltage transformer (SHVG)

AC4KV ±0.1KV

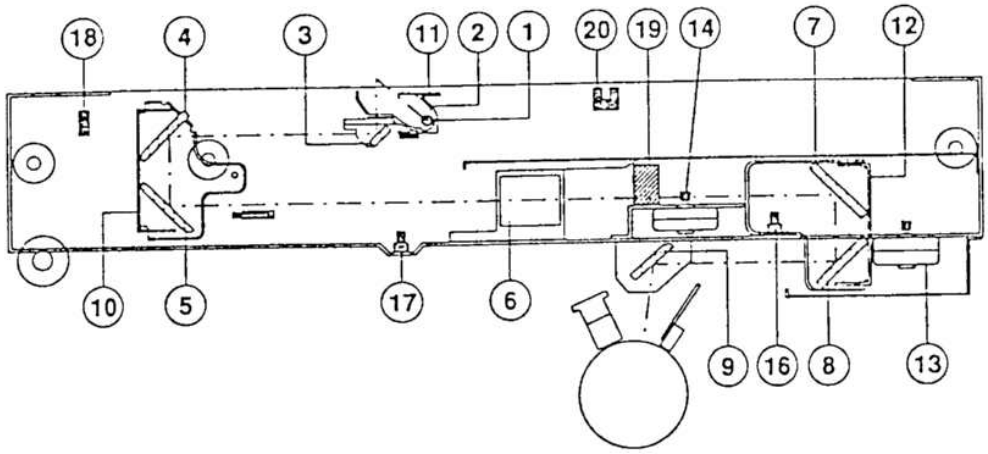
[10] OPTICAL SECTION

1. General

The SF-2022/2027 is composed of the fixed focus lens and six mirrors. The lens and the mirrors are moved by the stepping motor to positions according to the magnification ratio of reduction, normal, or enlargement copy. magnification ratio is changed from 0.5 to 2.0 in 151 steps by 1%. The six mirrors realizes a compact design. The slit exposure system with the moving light source is employed. Copy image density can be controlled by changing light quantity of the copy lamp.

The automatic exposure sensor is provided to sense density of th original and the copy lamp light quantity is controlled by the ma circuit to provide even copy image.

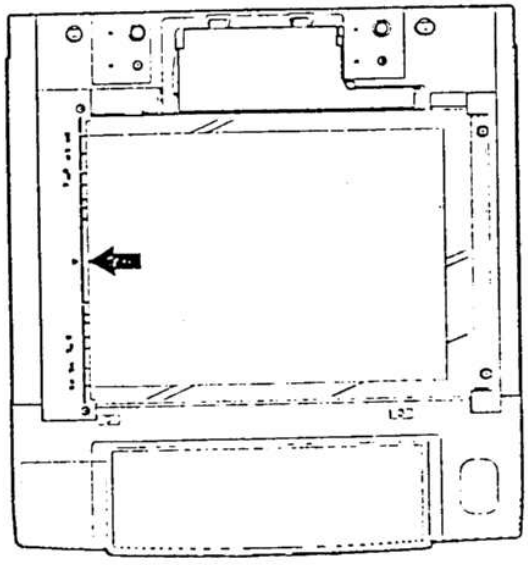
2. Basic composition



(1)	Copy lamp	(2)	Reflector	(3)	No. 1 mirror
(4)	No. 2 mirror	(5)	No. 3 mirror	(6)	Lens
(7)	No. 4 mirror	(8)	No. 5 mirror	(9)	No. 6 mirror
(10)	Mirror base B unit	(11)	Copy lamp unit	(12)	Mirror base C unit
(13)	Lens drive motor	(14)	No. 4, No. 5 mirror base drive motor	(15)	Mirror motor
(16)	Mirror base home position sensor	(17)	Lens home position sensor	(18)	Mirror home position sensor
(19)	Automatic exposure sensor	(20)	OC switch		

(1) Original table

The original table is fixed, and an original is set to the left center.



(2) Copy lamp

100V system 85V 275W
200V system 170V 310W

(3) Mirror

Six mirrors are used.
No. 1 mirror is attached to copy lamp unit, No. 2 and No. 3 mirrors to mirror base B, No. 4 and No. 5 mirrors to mirror base C.
Mirror bases A and B are scanned when copying. Mirror base C is used to change the distance between an original and the photoconductor in reduction or enlargement copy.

(4) Lens (Fixed focus lens)

- Construction: 1 group 3 lenses
- Brightness: F8.5
- Focal distance: 195mm ±1%

(5) Lens home position sensor (LHPS)

This sensor is used to sense lens position. The output signal c this sensor serves as the basic signal to control the copy mag.....ca tion ratio.

(6) No. 4, No. 5 mirror base home position sensor (MBHPS)

This sensor is used to sense mirror base C (No. 4, No. 5 mirrors). The output of this sensor serves as the basic signal to control the copy magnification ratio.

(7) Lens base

The lenses are mounted to this base, which is moved in the paper feed direction for reduction copy and in the paper exit direction for enlargement copy.

(8) Lens slide shaft

This shaft is used to control optical axis of the lenses in reduction or enlargement copy. The lenses follow on the slide base shaft.

(9) Lens drive wire

The lens drive wire is used to move the lens base.

(10) Mirror base C

No. 4 and No. 5 mirrors are attached to mirror base C. Mirror base C is moved by the mirror base drive motor to adjust the distance between an original and the photoconductor in reduction or enlargement copy.

(11) Mirror base C (No. 4, No. 5 mirrors) drive wire

This wire is used to move mirror base C (No. 4, No. 5 mirrors).

(12) Mirror motor

The mirror motor is a DC servo motor used to move mirror base A and mirror base B. Its rotation is adjusted according to each magnification ratio.

(13) Mirror home position sensor (MHPS)

This is a transmission type sensor used to sense the home position of mirror base A.

(14) Mirror base B

No. 2 and No. 3 mirrors ar attache to mirror base B, which is scanned by the mirror motor.

(15) Copy lamp unit

This is composed of No. 1 mirror, the thermal fuse, the copy lamp, the exposure adjusting plate, and the reflector, and is scanned by the mirror motor.

(16) Thermal fuse

The thermal fuse is provided at the reflector to prevent against abnormal temperature rise in the optical system. In case of an abnormal temperature rise, it turns off the power source of the copy lamp.
100V system 109 °C
200V system 109 °C

(17) Reflector

Light from the copy lamp is reflected by the reflector onto an original.

(18) Exposure adjusting plate

There are three exposure adjusting plates attached to mirror base A to adjust exposure balance between the front and the rear sides.

(19) Mirror base drive wire

The mirror motor power is transmitted to mirror base A and mirror base B to scan the mirror base by means of this wire.

(20) Mirror base (No. 4, No. 5) drive motor

This is a stepping motor used to drive mirror base C.

(21) Lens drive motor

This is a stepping motor used to change lens positions.

(22) AE sensor

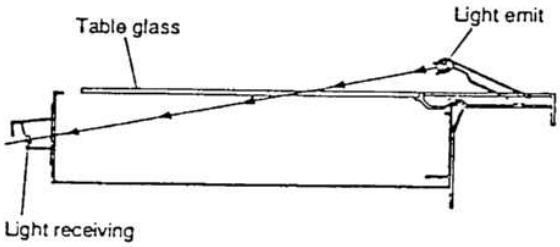
The AE sensor senses the original density by the magnitude of light reflected from the original. The center area of about 100mm wide in the mirror base scan direction is the light measuring area.
The elements are photo diodes.

(23) Blank lamp operation

When a reduction image is copied on a large size paper in reduction copy, the outside area becomes black background.
In another copy mode also, electric charges are remained on the outer area of the original image and toner is attracted to the area. To discharge this, light is radiated on the drum by the blank lamp to prevent against adhesion of toner in the outer area of the image.
The lead edge void is formed by the drum discharge system with the blank lamp light. The void width can be adjusted by the diagnostic function.

(24) Original size detection

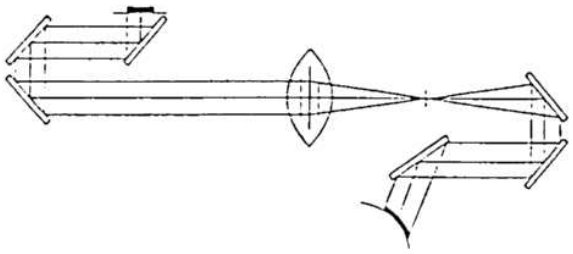
The original interruption system is employed, where light is passed from LED in the rear frame side through the table glass to the original to sense the original size.



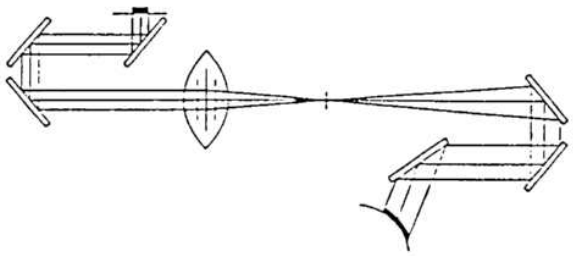
3. Basic operation

(Relation between an original, the lenses, and images in each magnification ratio)

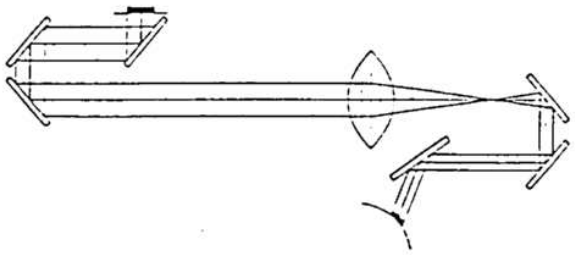
Normal copy: The distance between the original surface set on the table glass and the lens is adjusted to the distance between the lens and the exposure surface of the photoconductor to make a normal copy.

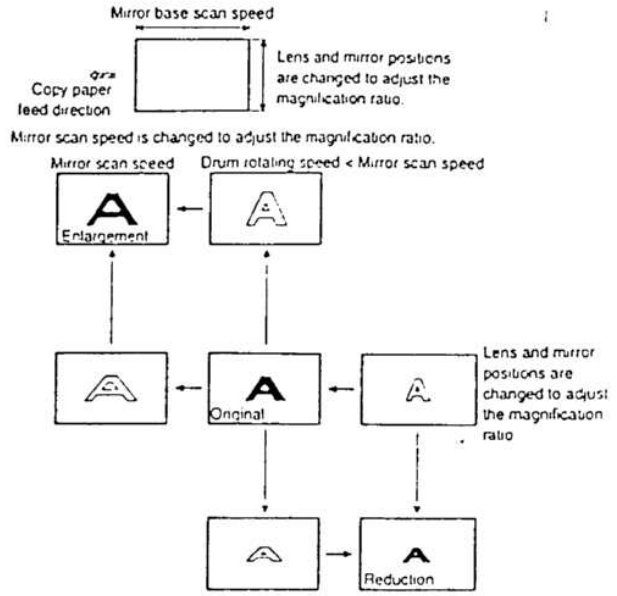


Enlargement: The lens approaches nearer the original compared from the normal copy and the distance between the original surface and the lens is shortened.
No. 4 and No. 5 mirrors go far from the lens and the distance between the lens and the exposure surface of the photoconductor becomes greater.
The distance between the original and the exposure surface of the photoconductor becomes greater than in the normal copy.



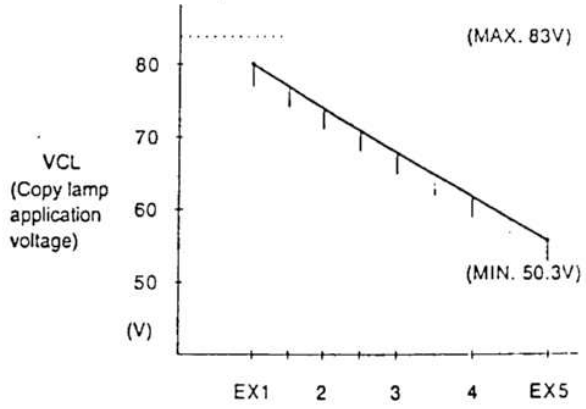
Reduction: The lens approaches nearer the photoconductor compared from the normal copy, and the distance between the original surface and the lens becomes greater.
The distance between the lens and the exposure surface of the photoconductor becomes shorter.
No. 4, 5 mirror and the mirror base go far from the lens.
The distance between the original and the exposure surface of the photoconductor becomes greater than in normal copy.





(Copy lamp control for each copy density mode)

- Manual density copy mode



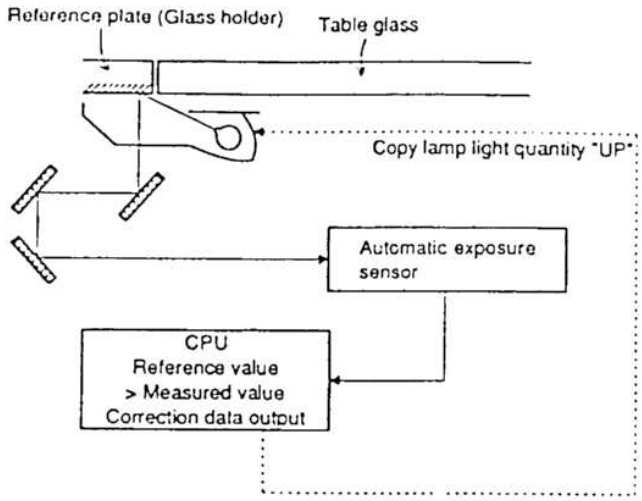
Perform simulation 46-01 to determine the copy lamp applica' tages (Vcl) in EX1 and EX5.
When the copy lamp application voltages in EX1.0 and EX5.0 ar determined, the voltage difference between them is divided into nine. The application voltage of the copy lamp at each exposure level is determined by changing ON time duty of the copy lamp ON contro signal.

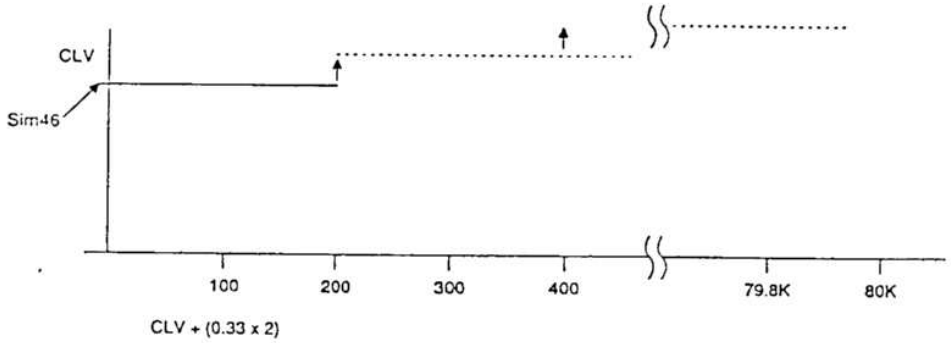
- Photo density copy mode

The control method is same as in the manual density copy mode. The image density is controlled by decreasing the grid bias voltage of the charging corona. To reproduce half tone image, however, ON time duty of the copy lamp ON signal is made shorter than in the manua density copy mode. (The application voltage is reduced.)

4. Optical system dirt correction

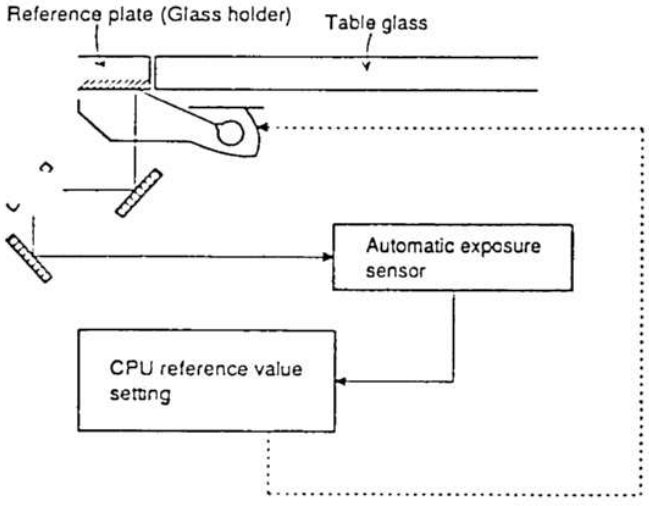
In SF-2022/2027, exposure density is corrected by changing the copy lamp light quantity depending on dirt in the optical system (the copy lamp unit, No. 1 mirror, No. 2 mirror, No. 3 mirror).
The optical system dirt correction is performed as follows:





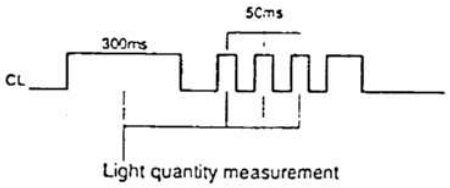
(1) Setting the reference value for optical system correction.

① Clean the optical system at every maintenance.



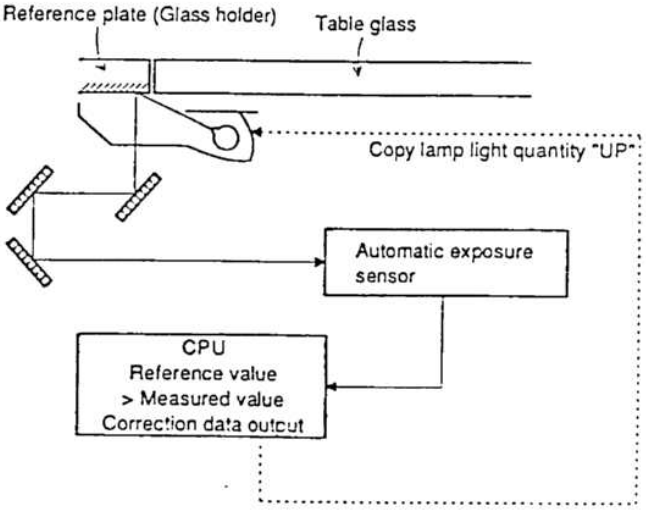
② Perform Simulation 46-1.
(The previous data are cleared.)

③ After completion of Simulation 46-1, when performing the first mirror initialization, measure light quantity of the copy lamp.



Obtain the average value from the four measurement values and use the average value as the reference value for correction.

(2) Dirt correction

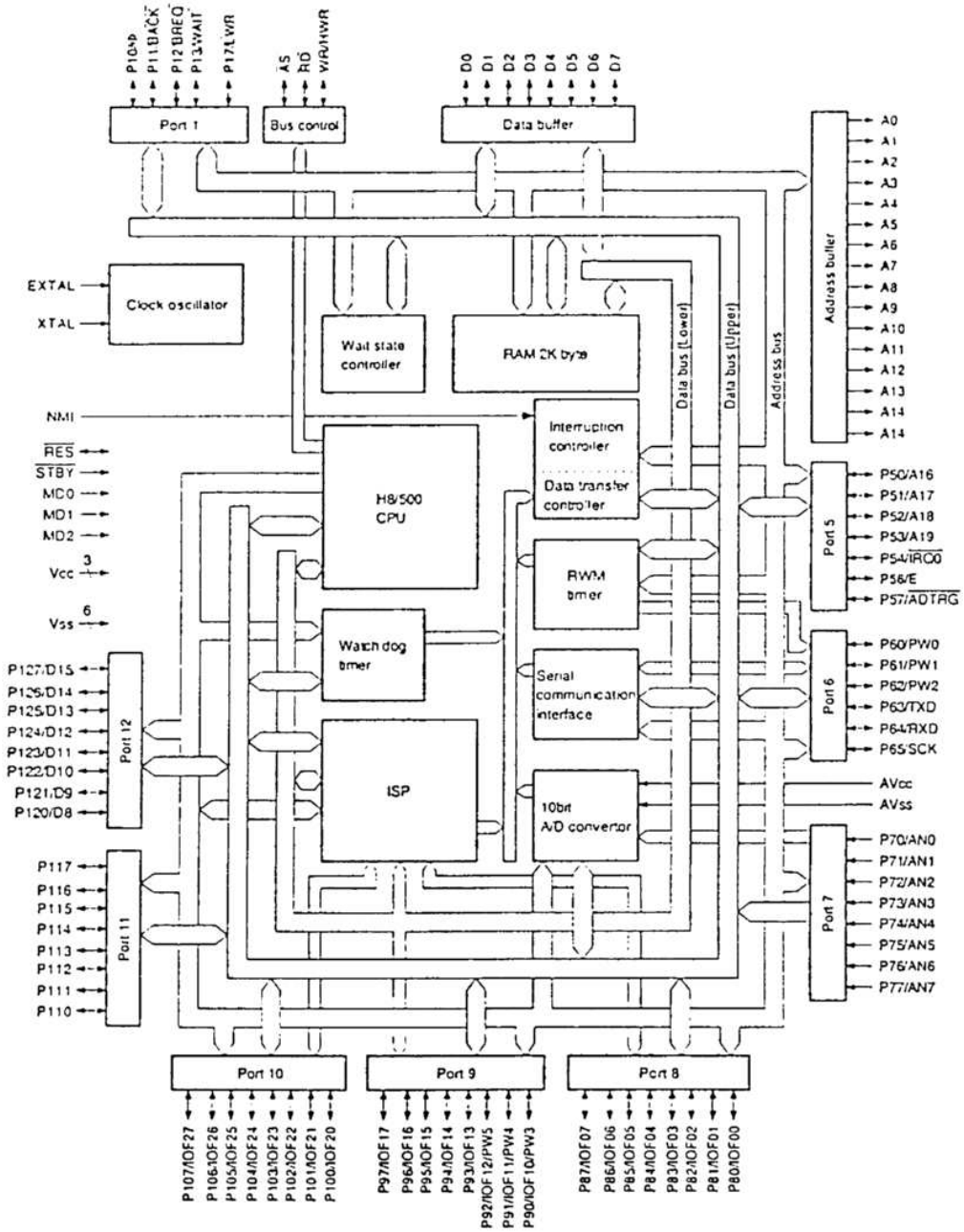


① Measure light quantity when performing mirror initialization.
If, however, the number in the digit of 100 is an odd number, only set the flags in the register inside the CPU and do not perform correction.
If the number in the digit of 100 is an even number and the flag in the register inside the CPU is set, perform light correction.

② Store the correction data into memory.

③ Reset the register inside the CPU.

4. Internal block diagram



⑤ CPU (IC113) pin signal

Pin No.	Port	Signal name	I/O	H.L	Specifications
1	P90	LEMT0	OUT	H	Lens motor drive signal A
2	P91	LEMT1	OUT	H	Lens motor drive signal B
3	P92	LEMT2	OUT	H	Lens motor drive signal -A
4	P93	LEMT3	OUT	H	Lens motor drive signal -B
5	P94	CLK	OUT	H	Clock signal for data output to BL.OPPWB
6	P95	DATA	OUT	H	Serial data output to BL.OPPWB
7	P96	BSPWM	OUT	H	High voltage unit bias level control pulse
8	P97	CLPWM	OUT	H	Copy lamp light quantity control pulse
9	VCC	+5V2			Power source (5V)
10	P100	FWS	IN	H	Power frequency detection signal (AC waveform zero cross timing)
11	P101	KEY	IN	H	Operation PWB key input signal (Serial data)
12	P102	NC			
13	P103	RE	IN	H	Pulse signal generated by mirror motor rotation
14	P104	$\overline{\text{MHPS}}$	IN	L	Optical unit home position sense signal
15	P105	NC			
16	P106	$\overline{\text{R-TXD}}$	OUT	L	Serial data output to RIC (Not used)
17	P107	$\overline{\text{R-RXD}}$	IN	L	Serial data input from RIC (Not used)
18	P80	PAM1-0	OUT	H	ADU side plate motor drive signal A
19	P81	PAM1-1	OUT	H	ADU side plate motor drive signal B
20	P82	PAM1-2	OUT	H	ADU side plate motor drive signal -A
21	P83	PAM1-3	OUT	H	ADU side plate motor drive signal -B
22	P84	MBMT0	OUT	H	Mirror base motor drive signal A
23	P85	MBMT1	OUT	H	Mirror base motor drive signal B
24	P86	MBMT2	OUT	H	Mirror base motor drive signal -A
25	P87	MBMT3	OUT	H	Mirror base motor drive signal -B
26	VSS	GND			Power source (GND)
27	P120	PAM2-0	OUT	H	ADU rear plate motor drive signal A
28	P121	PAM2-1	OUT	H	ADU rear plate motor drive signal B
29	P122	PAM2-2	OUT	H	ADU rear plate motor drive signal -A
30	P123	PAM2-3	OUT	H	ADU rear plate motor drive signal -B
31	P124	RRC	OUT	H	Resist roller clutch drive signal
32	P125	DCH	OUT	H	CPU reset signal
33	P126	TRCL	OUT	H	Transport roller clutch (low speed)
34	P127	TRCH	OUT	H	Transport roller clutch (high speed)
35	VSS	GND			Power source (GND)
36	D0	D0			Data signal
37	D1	D1			Data signal
38	D2	D2			Data signal
39	D3	D3			Data signal
40	D4	D4			Data signal
41	D5	D5			Data signal
42	D6	D6			Data signal
43	D7	D7			Data signal
44	VCC	+5V2			Power source (GND)
45	A0	A0			Address signal
46	A1	A1			Address signal
47	A2	A2			Address signal
48	A3	A3			Address signal
49	A4	A4			Address signal
50	A5	A5			Address signal
51	A6	A6			Address signal
52	A7	A7			Address signal
53	VSS	GND			Power source (GND)
54	A8	A8			Address signal
55	A9	A9			Address signal
56	A10	A10			Address signal

Pin No	Port	Signal name	I/O	H.L	Specifications
57	A11	A11			Address signal
58	A12	A12			Address signal
59	A13	A13			Address signal
60	A14	A14			Address signal
61	A15	A15			Address signal
62	A16	A16			Address signal
63	A17	A17			Address signal
64	A18	A18			Address signal
65	A19	A19			Address signal (Not used)
66	P13	R-DSR	IN		Data set ready signal from RIC
67	P12	$\overline{\text{APHPS2}}$	IN	L	ADU rear plate sense (L at HP) (Sensor pin, H at HP)
68	P11	$\overline{\text{APHPS1}}$	IN	L	ADU width sense (L at HP) (Sensor pin, H at HP)
69	P10	80	IN		Short signal for Simulation 80 input (Not used)
70	$\overline{\text{RES}}$	$\overline{\text{RESET}}$	IN	L	Reset state at LOW (0V).
71	NMI	POFA	IN	H	Low with stable power voltage.
72	VSS	GND			Power source (GND)
73	EXTAL	EXTAL	IN		Clock (8MHz)
74	XTAL	XTAL	IN		Clock (8MHz)
75	VCC	+5V2			Power source (5V)
76	$\overline{\text{AS}}$	NC			
77	$\overline{\text{RD}}$	$\overline{\text{RD}}$	OUT	L	ROM, RAM, I/O data read signal
78	$\overline{\text{WR}}$	$\overline{\text{WR}}$	OUT	L	ROM, RAM, I/O data write signal
79	P17	U2	IN		U2 trouble cancel short signal (Not used)
80	MD0	GND	IN	L	Operation mode, control signal
81	MD1	+5V2	IN	H	Operation mode, control signal
82	MD2	+5V2	IN	H	Operation mode, control signal
83	$\overline{\text{STBY}}$	+5V2	IN	H	Hardware standby mode signal
84	AVCC	AVCC			A/D convertor reference voltage pin
85	AN0	AES	IN		Analog input signal (AE sensor)
86	AN1	TH	IN		Analog input signal (Thermistor)
87	AN2	PWS	IN		Analog input signal (Manual feed paper width sense: not used)
88	AN3	TCSA	IN		Analog input signal (Toner concentration sensor)
89	AN4	PD	IN		Analog input signal
90	AN5	PC	IN		Analog input signal
91	AN6	PLS	IN		Analog input signal (Manual feed paper length sense: Not used)
92	AN7	AN7	IN		Analog input signal
93	AVSS	GND			A/D convertor ground pin
94	VSS	GND			Power source (GND)
95	P57	$\overline{\text{SMDIR}}$	OUT	L	Mirror motor feed return select signal
96	P56	NC			
97	P54	NC			
98	P60	SMPWM	OUT	H	Mirror motor speed control pulse
99	P61	$\overline{\text{MBHPS}}$	IN	L	No. 4/5 mirror home position sense signal (L at HP)
100	P62	$\overline{\text{LHPS}}$	IN	L	Lens home position sense signal (L at HP)
101	P63	$\overline{\text{TXD}}$	OUT	L	Serial data output to each slave CPU
102	P64	$\overline{\text{RXD}}$	IN	L	Serial data input from each slave CPU
103	P65	NC			
104	VSS	GND			Power source (GND)
105	P110	$\overline{\text{PPD1}}$	IN	L	Paper transport sensor 1
106	P111	$\overline{\text{PPD2}}$	IN	L	Paper transport sensor 2
107	P112	$\overline{\text{IN2}}$	IN		Switch sense strobe signal
108	P113	$\overline{\text{IN3}}$	IN		Switch sense strobe signal
109	P114	$\overline{\text{IN4}}$	IN		Switch sense strobe signal
110	P115	$\overline{\text{IN5}}$	IN		Switch sense strobe signal
111	P116	$\overline{\text{IN6}}$	IN		Switch sense strobe signal
112	P117	$\overline{\text{IN7}}$	IN		Switch sense strobe signal

(3) I/O (IC114) TE7750

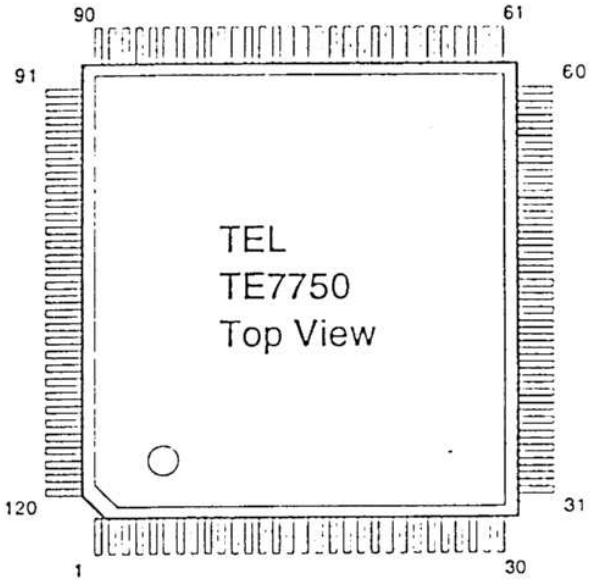
① General

The I/O converts output data of the CPU into the control signals.
The TE7750 is a versatile-use interface element.
Nine sets (8 bit) of I/O ports are provided to set I/O operations of parallel data by the program or the hardware.

② Features

8 bit parallel I/O ports (x 9 ports)

③ Pin arrangement



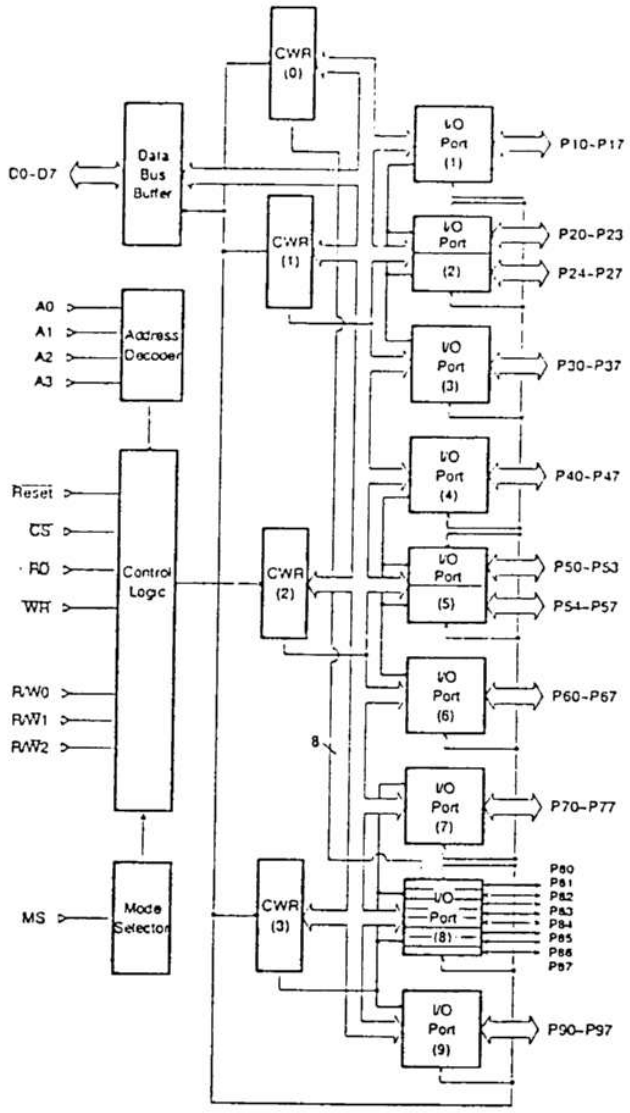
Pin	I/O	Pin name
1	—	VSS
2	—	NC
3	I	MS
4	I/O	P10
5	I/O	P11
6	I/O	P12
7	I/O	P13
8	I/O	P14
9	I/O	P15
10	I/O	P16
11	I/O	P17
12	I/O	P40
13	I/O	P41
14	—	VDD
15	—	VSS
16	I/O	P42
17	I/O	P43
18	I/O	P44
19	I/O	P45
20	I/O	P46
21	I/O	P47
22	I/O	P20
23	I/O	P21
24	I/O	P22
25	I/O	P23
26	I/O	P24
27	I/O	P25
28	—	NC
29	—	NC
30	—	NC

Pin	I/O	Pin name
31	—	VSS
32	—	NC
33	I/O	P26
34	I/O	P27
35	I/O	P50
36	I/O	P51
37	I/O	P52
38	I/O	P53
39	I/O	P54
40	I/O	P55
41	I/O	P56
42	I/O	P57
43	I/O	P30
44	—	VDD
45	—	VSS
46	I/O	P31
47	I/O	P32
48	I/O	P33
49	I/O	P34
50	I/O	P35
51	I/O	P36
52	I/O	P37
53	I/O	P70
54	I/O	P71
55	I/O	P72
56	I/O	P73
57	—	NC
58	—	NC
59	—	NC
60		P74

Pin	I/O	Pin name
61	—	VSS
62	—	NC
63	I/O	P75
64	I/O	P76
65	I/O	P77
66	I/O	P60
67	I/O	P61
68	I/O	P62
69	I/O	P63
70	I/O	P64
71	I/O	P65
72	I/O	P66
73	I/O	P67
74	—	VDD
75	—	VSS
76	I/O	P90
77	I/O	P91
78	I/O	P92
79	I/O	P93
80	I/O	P80
81	I/O	P81
82	I/O	P82
83	I/O	P83
84	I/O	P84
85	I/O	P85
86	I/O	P86
87	I/O	P87
88	—	NC
89	—	NC
90	—	NC

Pin	I/O	Pin name
91	—	VSS
92	—	NC
93	I/O	P94
94	I/O	P95
95	I/O	P96
96	I/O	P97
97	I	RW0
98	I	RW1
99	I	RW2
100	I/O	D0
101	I/O	D1
102	I/O	D2
103	I/O	D3
104	–	VDD
105	–	V
106	I/O	D4
107	I/O	D5
108	I/O	D6
109	I/O	D7
110	I	A0
111	I	A1
112	I	A2
113	I	A3
114	I	RD
115	I	WR
116	I	CS
117	—	NC
118	—	NC
119	—	NC
120	I	RESET

(4) Internal block diagram



(5) I/O (IC114) pin signal

Pin No.	Port	Signal name	I/O	H/L	Specifications
1	VSS	GND			Power source (GND)
2	NC				
3	MS	+5V2	IN	H	Mode select (Hard mode (2) at H)
4	P10	LATCH-OP	OUT	H	Latch signal of output data to the operation PWB
5	P11	LATCH-BL	OUT	H	Latch signal of output data to BL PWB
6	P12	ASEL0	OUT		TXD, DTR output select signal
7	P13	ASEL1	OUT		TXD, DTR output select signal
8	P14	BEO-OP	OUT	H	Operation PWB output driver ON/OFF control signal
9	P15	BEO-BL	OUT	H	BL PWB output driver ON/OFF control signal
10	P16	NC			
11	P17	NC			
12	P40	AEG0	OUT	H	AE GAIN select signal
13	P41	AEG1	OUT	H	AE GAIN select signal
14	VDD	+5V2			Power source (5V)
15	VSS	GND			Power source (GND)
16	P42	AEG2	OUT	H	AE GAIN select signal
17	P43	SRES	OUT	H	Slave PWB reset signal (Not used)
18	P44	TMa	OUT	H	Toner supply motor drive signal
19	P45	TMb	OUT	H	Toner supply motor drive signal
20	P46	NC			
21	P47	NC			
22	P20	DTR	OUT		Data transmit ready signal
23	P21	DPFC	OUT	H	Duplex tray paper feed clutch drive signal
24	P22	CLE	OUT	H	Copy lamp enable signal (ON at H)
25	P23	AUDCL	OUT	H	Auditor time-out clear
26	P24	AUDCP	OUT	H	Auditor during copy cycle
27	P25	PNC	OUT	H	Personal counter control signal
28	NC				
29	NC				
30	NC				
31	VSS	GND			Power source (GND)
32	NC				
33	P26	LED0	OUT	H	Original size sense LED lighting signal
34	P27	LED1	OUT	H	Original size sense LED lighting signal
35	P50	MHV	OUT	H	Main corona high voltage output control signal
36	P51	THV	OUT	H	Transfer corona high voltage output control signal
37	P52	SHV	OUT	H	Separation corona high voltage output control signal
38	P53	EX1	OUT	H	Reserved.
39	P54	GR SEL0	OUT	H	Grid bias control signal 0
40	P55	GR SEL1	OUT	H	Grid bias control signal 1
41	P56	DDC	OUT	H	Duplex drive connection clutch
42	P57	PR	OUT	H	Power relay control signal
43	P30	VFM1	OUT	H	Ventilation fan motor control signal 1
44	VDD	+5V2			Power source (5V)
45	VSS	GND			Power source (GND)
46	P31	VFM2	OUT	H	Ventilation fan motor control signal 2
47	P32	DRRC	OUT	H	Duplex reversion roller clutch
48	P33	MM	OUT	H	Main motor control signal
49	P34	SFM	OUT	H	Suction fan motor control signal
50	P35	MPFS	OUT	H	Manual paper feed solenoid control signal
51	P36	CPFS1	OUT	H	Upper cassette paper feed solenoid control signal
52	P37	CPFS2	OUT	H	Lower cassette paper feed solenoid control signal
53	NC				
54	P71	CPFC1	OUT	H	Upper cassette paper feed clutch control signal
55	P72	CPFC2	OUT	H	Lower cassette paper feed clutch control signal
56	P73	MMPR	OUT	H	Main motor power relay control signal
57	NC				
58	NC				
59	NC				
60	P74	HL	OUT	H	Heater lamp control signal
61	VSS	GND			Power source (GND)

Pin No	Port	Signal name	I/O	H/L	Specifications
62	NC				
63	P75	LUM1	OUT	H	Lift up motor control signal (upper stage)
64	P76	LUM2	OUT	H	Lift up motor control signal (lower stage)
65	P77	PSPS	OUT	H	Paper separation solenoid control signal
66	P60	W0	OUT	H	Switch sense strobe signal
67	P61	W1	OUT	H	Switch sense strobe signal
68	P62	W2	OUT	H	Switch sense strobe signal
69	P63	W3	OUT	H	Switch sense strobe signal
70	P64	W4	OUT	H	Switch sense strobe signal
71	P65	W5	OUT	H	Switch sense strobe signal
72	P66	W6	OUT	H	Switch sense strobe signal
73	NC				
74	VDD	+5V2			Power source (5V)
75	VSS	GND			Power source (GND)
76	P90	DGS	OUT	H	Duplex gate solenoid control signal
77	P91	CFM	OUT	H	Cooling fan motor control signal
78	P92	SSEL	OUT		OP.BL select signal
79	NC				
80	P80	PLED	OUT	H	Process control LED (Not used)
81	P81	R-RTS	OUT		RTS for RIC (Not used)
82	P82	R-DTR	OUT		DTR for RIC (Not used)
83	P83	SME	OUT	L	Mirror motor enable signal (ON at L)
84	NC				
85	NC				
86	NC				
87	NC				
88	NC				
89	NC				
90	NC				
91	VSS	GND			Power source (GND)
92	NC				
93	P94	$\overline{\text{POSEL0}}$	OUT	L	Original sense photo transistor select signal
94	P95	$\overline{\text{POSEL1}}$	OUT	L	Original sense photo transistor select signal
95	P96	$\overline{\text{POSEL2}}$	OUT	L	Original sense photo transistor select signal
96	P97	DL	OUT	H	Discharge lamp control signal
97	PW0	$\overline{\text{L(GND)}}$	IN	L	Read/write set signal
98	RW1	$\overline{\text{L(GND)}}$	IN	L	Read/write set signal
99	RW2	$\overline{\text{L(GND)}}$	IN	L	Read/write set signal
100	D0	D0	IN		Data signal
101	D1	D1	IN		Data signal
102	D2	D2	IN		Data signal
103	D3	D3	IN		Data signal
104	VDD	+5V2			Power source (5V)
105	VSS	GND			Power source (GND)
106	D4	D4	IN		Data signal
107	D5	D5	IN		Data signal
108	D6	D6	IN		Data signal
109	D7	D7	IN		Data signal
110	A0	A0	IN		Address signal
111	A1	A1	IN		Address signal
112	A2	A2	IN		Address signal
113	A3	A3	IN		Address signal
114	RD	$\overline{\text{RD}}$	IN	L	Data read signal
115	WR	$\overline{\text{WR}}$	IN	L	Data write signal
116	CS	$\overline{\text{I/O CS}}$	IN	L	Chip select signal
117	NC				
118	NC				
119	NC				
120	RESET	$\overline{\text{RESET}}$	IN	L	Reset signal. Reset to initial state at LOW level of initial setting pulse input pin.

(4) RAM (IC115) X28C64

① General

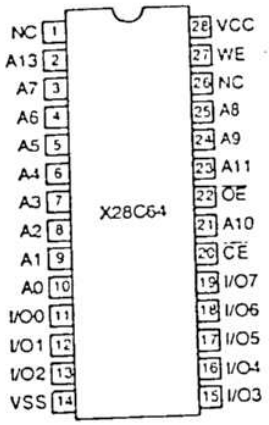
The RAM stores various set data necessary for the SF-2022/2027 system operations and counter data such as paper jam causes or trouble codes (without batteries). After turning on/off the power, data are transmitted between the RAM and the main CPU.
The X28C64 is an 8KByte EEPROM (Electrically Erasable PROM) and operates on a single power of 5V.

② Features

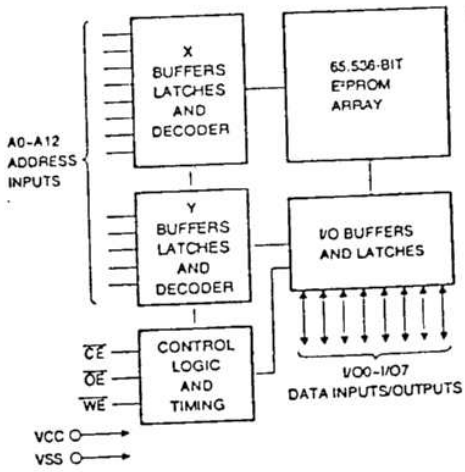
Low power CMOS operating current: Max. 60mA
All memory write time: Average 0.625sec

③ Pin arrangement

PLASTIC
CERDIP
FLAT PACK



④ Internal block diagram



⑤ RAM (IC115) pin signal

Pin No.	IN/OUT	Signal name	Function
1	—	nc	
2	IN	A12	Address signal
3 ~ 10	IN	A7 ~ A0	Address signal
11 ~ 13	IN/OUT	I/O0 ~ I/O2	Data signal
14	—	GND	GND (0V)
15 ~ 19	IN/OUT	I/O3 ~ I/O7	Data signal
20	IN	$\overline{CS}$	RAM chip select signal. RAM is selected at LOW (0V).
21	IN	A10	Address signal
22	IN	$\overline{RD}$	Read signal. RAM data are read into CPU at LOW level.
23	IN	A11	Address signal
24	IN	A9	Address signal
25	IN	A8	Address signal
26	IN	NC	
27	IN	$\overline{WR}$	Write signal. Data are written from CPU to RAM at LOW level (0V).
28	—	5V	Power source

6 Backup data list

Item	Set program No.	Content
Counter	20-01	Maintenance preset counter setting
	20-02	Domestic mini maintenance setting for black copy kit
	20-03	Domestic mini maintenance setting for color copy kit
	—	Maintenance counter
	—	JAM memory (Max. 50 pcs.)
	—	Total JAM counter
	—	Total counter
	—	Mini maintenance counter (3 colors)
	—	Mini maintenance preset counter
	—	RADF (ADF) counter
	—	ADU counter
Simulation set value	25-02	Automatic developer adjustment value
	26-01	Option setting
	26-03	Counter mode setting/Timer automatic clear setting
	26-06	Destination setting
	26-07	Drum sensitivity setting
	26-08	Lens focus setting
	26-09	No. 4/5 mirror characteristics setting
	26-10	DPCM SEC mode setting
	41-02	Original size sensor adjustment
	43	Fusing temperature setting
	46-01	Exposure level adjustment
	46-02	Exposure adjustment (Formula)
	47	AE sensor characteristics measurement
	48-01	Front/rear magnification ratio adjustment
	48-02	Paper transport direction magnification ratio adjustment
	50-01	Lead edge image position adjustment
	50-02	Lead edge image position adjustment
	51-02	Resist quantity adjustment
	51-05	Frame erase adjustment
	52-01	ADU alignment plate adjustment value setting
	52-02	ADU rear plate adjustment value setting
	53-01	RADF stop position adjustment (normal paper, one side)
	53-02	RADF stop position adjustment (normal paper, both sides)
	53-03	RADF stop position adjustment (thin paper)
	53-04	RADF resist sensor adjustment
	53-05	RADF reverse sensor adjustment

(5) Decoder (IC139, IC138)

① General

IC139 and IC138 are two sets of independent binary-quaternary decoders.

IC139A:

Enable	Select		Output		
GND	A17	A18	ROMCS	$\overline{\text{DOCS}}$	$\overline{\text{EEPROMCS}}$
L	L	L	L	H	H
L	H	L	H	L	H
L	L	H	H	H	L

Chip select signal is outputted with address data (A17, 18).

IC139B:

Enable	Select		Output			
$\overline{\text{DTR}}$	ASEL0	ASEL1	$\overline{\text{A-DTR}}$	$\overline{\text{D-DTR}}$	$\overline{\text{S-DTR}}$	$\overline{\text{O-DTR}}$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

Data receive enable signal from the slave CPU is outputted by address selector (ASEL0, 1).

$\overline{\text{A-DTR}}$: Data send enable from RADF/ADF

$\overline{\text{D-DTR}}$: Data send enable from the desk unit

$\overline{\text{S-DTR}}$: Data send enable from the sorter unit

$\overline{\text{O-DTR}}$: Data send enable from the operation PWB unit

IC138A:

Enable	Select		Output	
$\overline{\text{CLK}}$	SSEL	GND	CLK-OP	CLK-BL
L	L	L	L	H
L	H	L	H	L

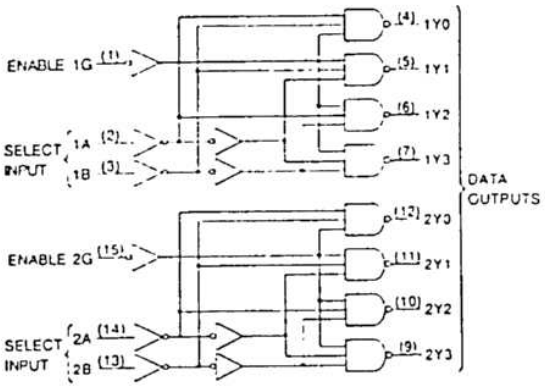
With select signal (SSEL), clock signal is outputted to the driver IC in the operation PWB and the blank lamp PWB.

IC138B:

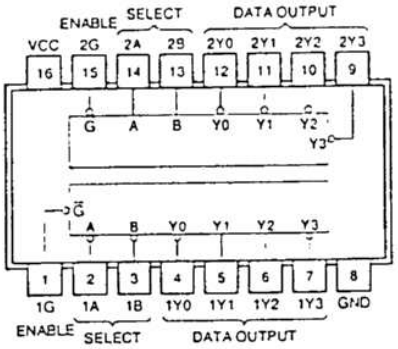
Enable	Select		Output			
$\overline{\text{TXD}}$	ASEL0	ASEL1	$\overline{\text{A-TXD}}$	$\overline{\text{D-TXD}}$	$\overline{\text{S-TXD}}$	$\overline{\text{O-TXD}}$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

With address selector (ASEL0, 1), the destination of the CPU output data is selected and the data are outputted.

② Internal logic diagram



③ Pin connection



④ Operations

When this is used as a decoder, if input 1A and 1B are specified with 2-bit binary codes, one of the outputs corresponding to the value becomes LOW and the other three outputs become HIGH. At the time, enable input E (15 pin, 1 pin) is kept at LOW. When E (15 pin, pin) is HIGh, all outputs become HIGH regardless of DA and DB.

1G	1B	1A	1Y0	1Y1	1Y2	1Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Note 1: X: HIGH or LOW.

(6) Start/stop control circuit

General

The circuit senses ON/OFF state of the power source to control start/stop of the circuits.
The DC power PWB supplies power voltages (VB=+24V, VC=+10V, VD1=5V, VD2=5V).
After the power voltage reaches the specified level, the circuit operation is started. Before the power voltage falls below the specified level, the circuit operation is stopped, preventing against malfunctions.

2 Operation

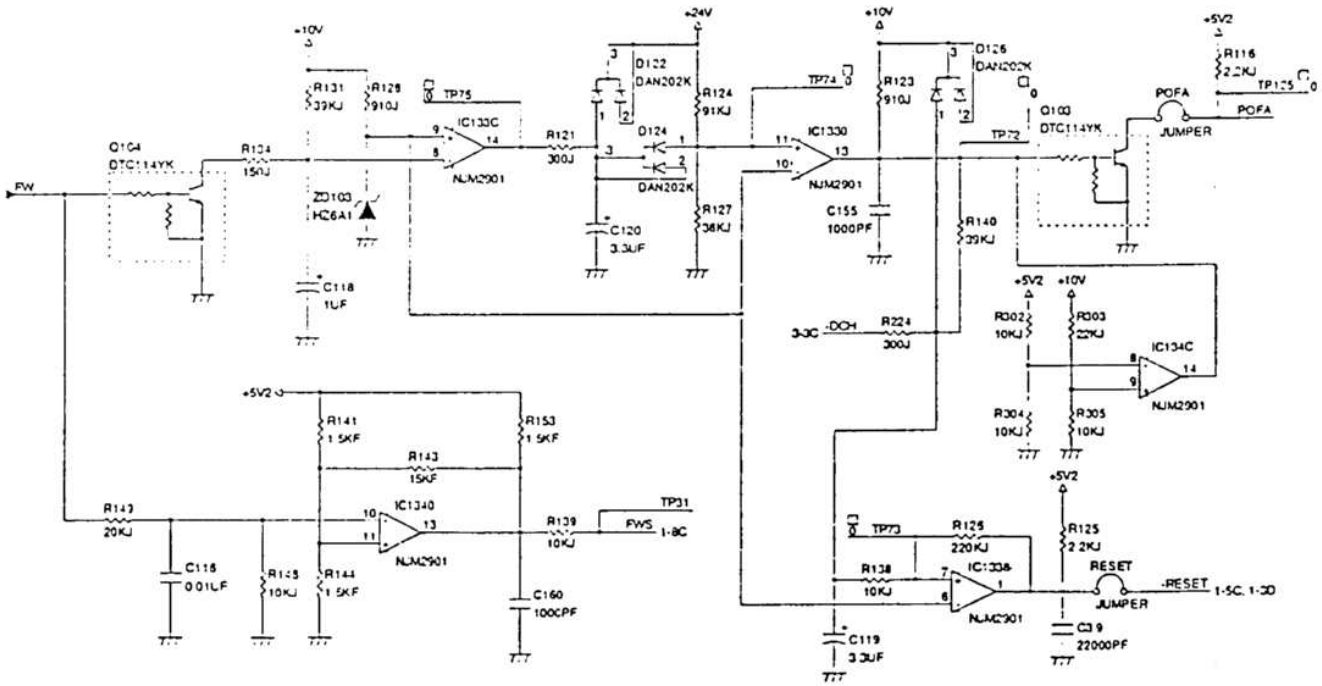
A. POFA generating circuit (Power voltage sense circuit)

This circuit senses ON/OFF of the power source and the power voltage. The DC power voltage is unstable immediately after turning on the power, or when the AC input voltage is abnormally low, or in the transition period after turning off the power.

When the DC voltage falls below the specified level, the circuits do not work properly. Especially when the power is turned on/off, data transmission is performed between the EEPROM (IC115) and the CPU (IC113). If, in this case, VD (+5V) power voltage if low, data transmission is not performed properly.

To protect against this malfunction, on/off of the power is sensed by this circuit and informed to the CPU so that the CPU starts data transmission with the RAM and the operations of each circuit and that it completes data transmission with the EEPROM and stops the operations of each circuit before the DC power voltage falls below the machine operation disable level. (Data transmission between the CPU and the EEPROM is allowed if only VD2 (+5V2) does not fall.)

Signal POFA is used to inform the CPU of on/off of the power and the DC power voltage state. POFA is driven HIGH to turn off the power when the DC power voltage becomes higher than the specified level. POFA is driven LOW just before the DC power voltage becomes low (0V).

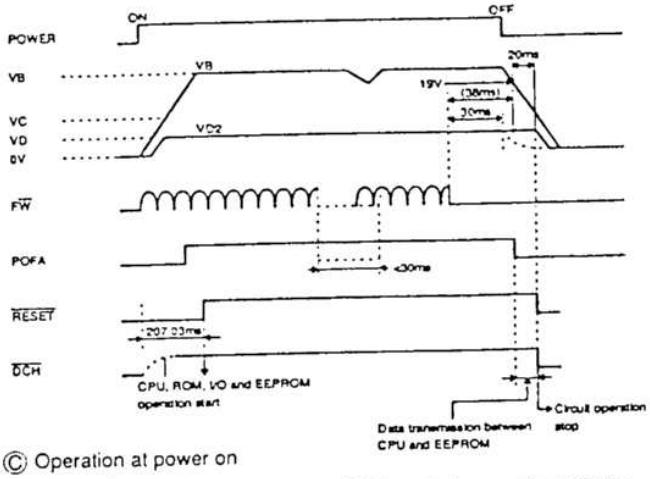


Ⓑ $\overline{\text{RESET}}$ generating circuit

$\overline{\text{RESET}}$ signal is formed with the power voltage sense signal (POFA) and the data transmission complete signal ($\overline{\text{DCH}}$) outputted from the CPU, and is used to operate each circuit in the stable range of the DC power voltage.

$\overline{\text{RESET}}$ signal is set (operation enabled) when POFA becomes HIGH (+5V), and is reset (operation stopped) when $\overline{\text{DCH}}$ becomes LOW (0V).

When POFA becomes LOW, data are transmitted from the CPU to the EEPROM. After completion of the data transmission, $\overline{\text{DCH}}$ becomes LOW.



Ⓒ Operation at power on

- When the power is turned on, FW rises to turn on the collector and the emitter of Q104 so that IC133 8 pin voltage becomes about 0.736V which is lower than 9 pin voltage (ZD103 5.2 ~ 5.5V). As a result, 14 pin is opened.
- 24V rises about 16msec after FW rising. C124 is charged through R124 and D124. IC133 5 pin voltage becomes higher than the reference voltage IC133 4 pin (ZD103 5.2 ~ 5.5V) in about 95msec so that 2 pin (POFA) becomes high.

Ⓓ Operation at power off

- When the power is turned off, FW falls to open the collector and the emitter of Q104. C118 is charged through R131. IC133 8 pin voltage becomes higher than 9 pin (ZD103 5.2 ~ 5.5V) in about 30msec. As a result, 14 pin becomes low.
- When IC133 14 pin becomes low, C120 is discharged and 5 pin voltage becomes about 0.8V which is lower than 4 pin (ZD103 5.2 ~ 5.5V). As a result, 2 pin (POFA) becomes low.

Ⓔ Operations at an instantaneous service interruption

Since POFA signal is outputted by IC133, it may erroneously outputted by discrepancy of resign times of 5V and 10V. To prevent against this, power voltages of 5V and 10V are monitored by R302, 303, 304, 305, and IC133.

- When the power is turned off, POFA should be driven low (0V) at the early stage. If it is driven low too early, however, the machine stops its operation even at an instantaneous service interruption (less than 30msec) which will not obstruct machine operation in normal cases. Therefore, off state of AC power for more than 30msec is judged as power OFF in this circuit and $\overline{\text{POFA}}$ is driven low.
- In normal operations, IC133 8 pin is at LOW level. At an instantaneous service interruption, FW becomes LOW to open the collector and the emitter of Q104, charging C118 through R131. So it takes more than 30msec for IC133 8 pin voltage to rise above the reference voltage (IC133 9 pin, 5.2V ~ 5.5V), and the machine does not stop at an instantaneous service interruption of 30msec or less.

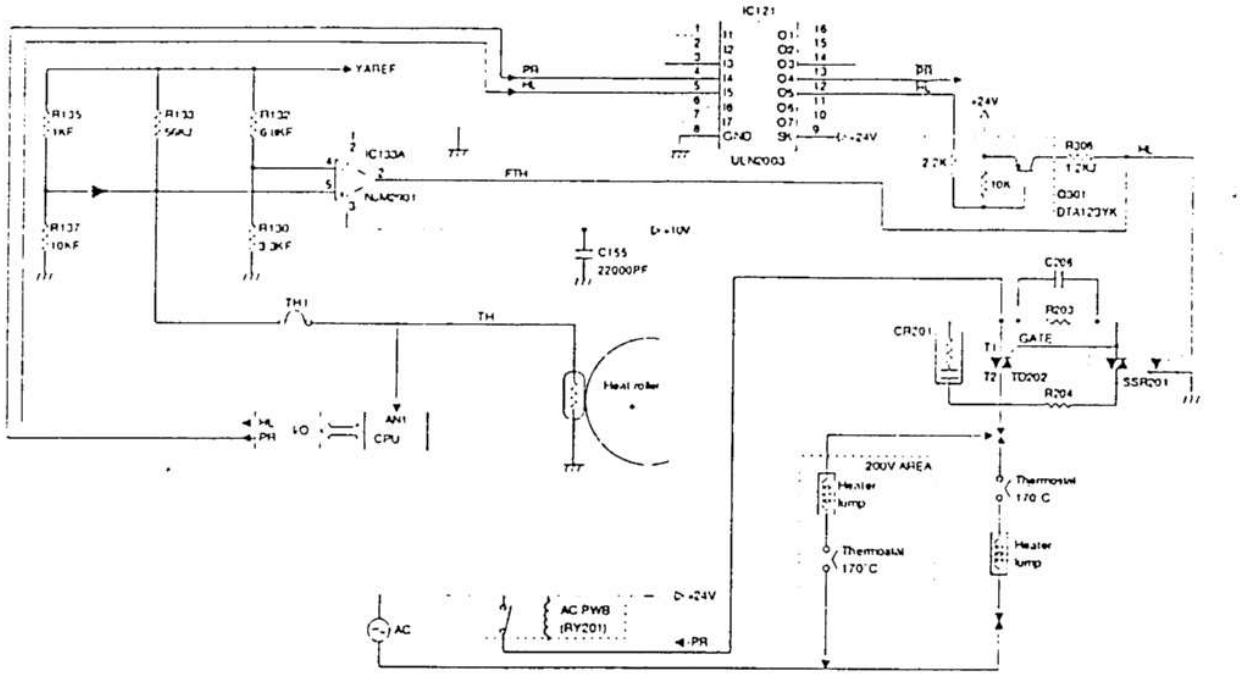
Ⓕ Operations when the power voltage falls

- When the AC power voltage falls below a certain leve D power voltage also falls though the DC power circ. is regulator circuit.
  Therefore, 24V is monitored and when it falls to 19V, $\overline{\text{POFA}}$ driven low (0V). (When it falls below 19V, IC133 5 pin voltag becomes lower than 4 pin reference voltage because of voltag division by R124 and R127. As a result, the output of com parator (IC133) becomes low.)

(7) Heater lamp control circuit

General

The heater lamp control circuit detects the heat roller surface temperature with the thermistor, converts it into voltage level, and outputs it to the CPU analog input pin.
The CPU converts the analog voltage into digital signal level, compares it with the value set by test commands, turns on/off the heater lamp according to the level, and maintain the heat roller surface temperature at a constant level.
When a paper jam occurs in the SF-2022/2027, this control circuit operates for max. 3 min to shorten the jam recovery time (8 sec).



When the heat roller surface temperature is low, the thermistor resistance increases. When the surface temperature is high, the resistance decreases. The thermistor terminal voltage, therefore, increases when the heat roller surface temperature is low, and decreases when the temperature is high. The thermistor terminal voltage is inputted to the CPU analog port, and the CPU controls on/off of the heater lamp with the input voltage level.

[High temperature protecting circuit in wild run of the CPU]

The voltage at IC133 3 pin (reference voltage) is divided by R130 and R132, and the thermistor terminal voltage is applied to IC133 2 pin. When 2 pin voltage is lower than 3 pin voltage (the heat roller surface temperature: about 230 degree C), output pin 1 becomes HIGH and IC133 2 pin becomes LOW. As a result, HL signal is pulled to the GND level and the heater lamp lighting signal is not generated. (IC133 output 2 pin is normally HIGH (Open state).)

[When the heat roller surface temperature is lower than the set temperature]

a. Since the thermistor pin voltage is higher than the set level, output signal HL from the CPU becomes HIGH.

b. HL signal is passed through IC121, TR, and Q301 to the solid state relay.
When, therefore, HL signal is LOW, the internal triac turns on.

c. When the internal traic turns on, a pulse is applied to the gate of the external triac to allow a current to flow from the power source rough the heater lamp to the triac, thus lighting the heater lamp.

[When the heat roller surface temperature is higher than the set temperature]

a. Since the thermistor pin voltage is lower than the set level, output signal HL from the CPU becomes low.

b. HL becomes low, SSR is turned off, the external triac is turned off, and the heater lamp is turned off.

[Q301]

Q301 protects the heater lamp from lighting due to trouble in the harness of the heater lamp drive signal.

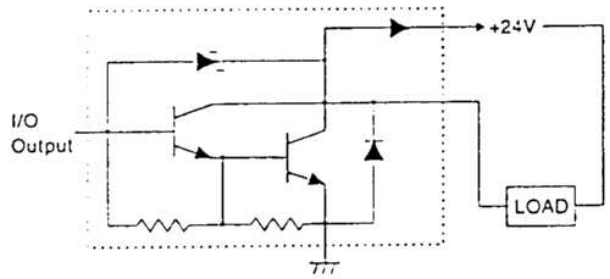
(8) Driver circuit (Solenoid, magnetic clutch)

① General

The control signals of each load outputted from the CPU and I/O cannot drive the load directly. The output, therefore, is delivered to the load through the driver IC.

② Operation

The driver circuit forms a Darlington circuit with two transistors to obtain a large drive current (load current) from a small input current (I/O output current). When the driver input voltage is HIGH (+5V), the transistor is turned on to flow a current in the arrow direction, operating the load. When the driver is turned on, the driver output pin voltage is 0V.

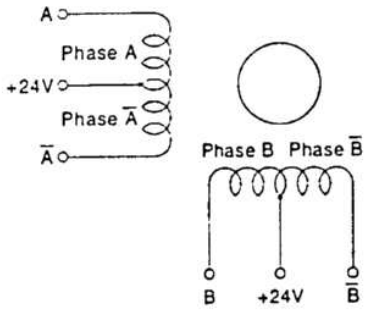


(9) Stepping motor drive circuit

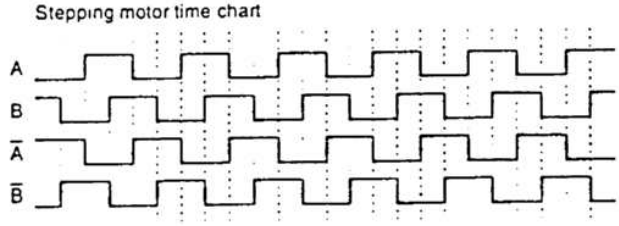
① General

The driver circuit drives the lens drive motor, the mirror base drive motor, the automatic duplex copy tray, the side plate motor, and the rear plate motor.

A: Stepping motor phase A coil drive signal
B: Stepping motor phase B coil drive signal
A: Stepping motor phase A coil drive signal
B: Stepping motor phase B coil drive signal



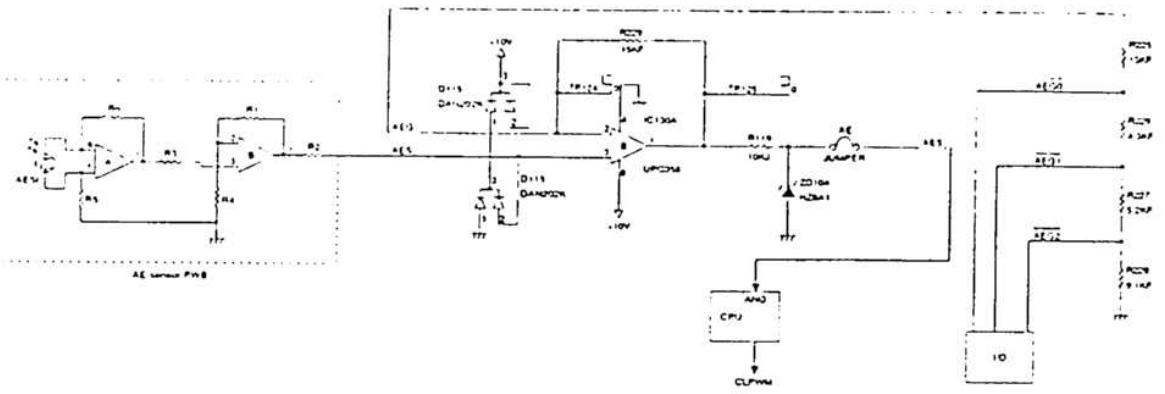
Stepping motor time chart



Drive signal	Lens drive	Mirror base drive	For Side plate	For rear plate
A	LEMT0	MBMT0	PAM1-0	PAM2-0
B	LEMT1	MBMT1	PAM1-1	PAM2-1
C	LEMT2	MBMT2	PAM1-2	PAM2-2
B	LEMT3	MBMT3	PAM1-3	PAM2-3

(10) AE (Auto Exposure) sensor circuit

AE circuit is composed of the AE sensor PWB which is comd of the photo diode, the I-V convertor circuit, and the amplifier circuit, and the amplifier circuit on the control PWB.



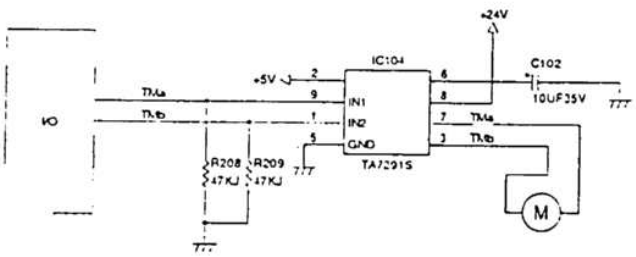
Operation amplifier A performs I-V conversion of the original density level (minute current) from the sensor. Operation amplifiers B and C nlify the output of operation amplifier A to a suitable level for ing to the CPU.

The amplifying level is automatically set by selecting the AE gain signal ($\overline{AEG0}$ ~ $\overline{AEG2}$) outputted from the I/O chip when test command SIM 47 is executed.

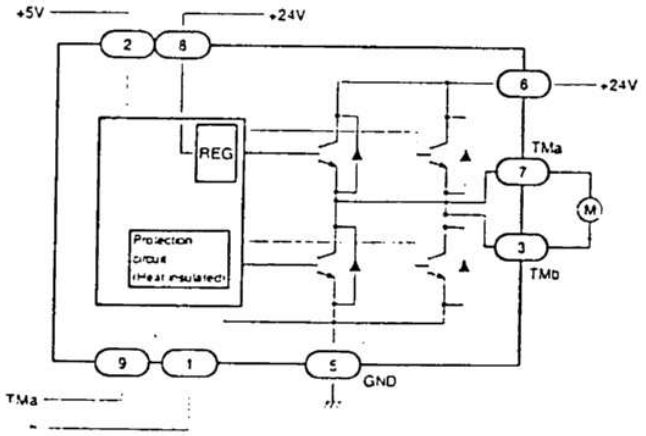
AE operation is performed by the software in the control PWB. When a reflected ray enters the sensor, a voltage corresponding to the light quantity is inputted to the CPU. The CPU compares the input voltage and the copy lamp application voltage and controls the copy lamp voltage so that the exposure level corresponds to the original density.

(11) Toner supply motor drive circuit

IC104 is the motor control IC which drives the toner supply motor with the pulse signals (TMa, TMb) outputted from the I/O chip.



Internal circuit



Truth value table

Input		Output		Mode
TMa	TMb	TMa	TMb	
L	L	∞	∞	Stop
H	L	H	L	CW/CCW
L	H	L	H	CCW/CW
H	H	L	L	Brake

∞ : High impedance

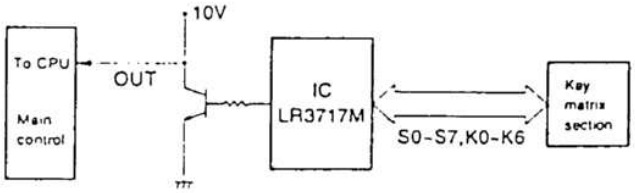
3. Operation circuit

General

- The operation circuit is composed of the key matrix circuit and the display circuit.

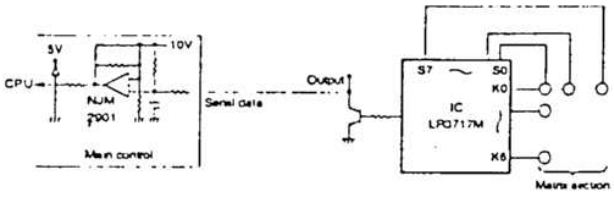
<Key circuit>

(1) Block diagram

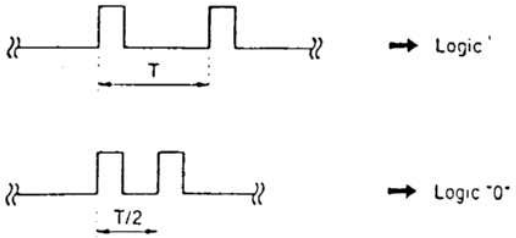


(2) Key detection

Key detection is performed by the key detection IC (LR3717M) with matrix of S0 ~ S7 and K0 ~ K6. Information is set to the CPU by serial data transmission. (8 x 8 matrix available)



The transmission system is PPM (Pulse Position Modulation) system using 15 bit data pulse signals.
The PPM transmission makes distinction of pulse width as logic "1" or logic "0."



As shown above, when the pulse interval is T, the pulse is judged a logic "1," and when the pulse interval is T/2, it is judged as logic "0
Pulse signals of 15 bits are serially sent.
PPM signal is judged from pulse interval "t" as shown below:

When t < 0.4 m : Abnormal
When 0.4 ms < t < 1.6 ms: "0"
When 1.6 ms < t < 3.2 ms: "1"
When 3.2 ms < t : Abnormal

When any abnormal signal enters the circuit, all the bits are cleared. Then the operation starts from the first bit again.
When data of more than 16 bits (17 pulse or more) are inputted, it is judged as an abnormal signal and all the bits are cleared. Then the operation begins from the first bit again.
The 15 bit data assignment is as shown below:

(A) System address (Refer to *1.) C1, C2, C3, C4, C5
These data are set with the switches and assigned depending on the system. 56 channels and 2 bit expansion are available for sending commands for one system.

*1: System address
This bit is set to prevent against malfunction in wireless communication with other devices (VTR, TV, etc.). For this time communication is made through wires and there is no need to set this bit. Set to "0."

(B) Data C6, C7, C8, C9, C10, C11
These data are assigned with the key input. Commands corresponding to C6 ~ C11 are as shown below:

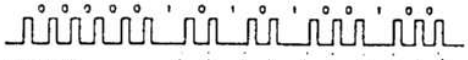
C6	C7	C8	C9	C10	C11	CH	C6	C7	C8	C9	C10	C11	CH	C6	C7	C8	C9	C10	C11	CH	C6	C7	C8	C9	C10	C11	CH
1	0	0	0	0	0	1	0	0	0	0	1	0	16	1	1	1	1	1	0	31	0	1	1	1	0		5
0	1	0	0	0	0	2	1	0	0	0	1	0	17	0	0	0	0	0	1	32	1	1	1	1	0	1	47
1	1	0	0	0	0	3	0	1	0	0	1	0	18	1	0	0	0	0	1	33	0	0	0	0	1	1	48
0	0	1	0	0	0	4	1	1	0	0	1	0	19	0	1	0	0	0	1	34	1	0	0	0	1	1	49
1	0	1	0	0	0	5	0	0	1	0	1	0	20	1	1	0	0	0	1	35	0	1	0	0	1	1	50
0	1	1	0	0	0	6	1	0	1	0	1	0	21	0	0	1	0	0	1	36	1	1	0	0	1	1	51
1	1	1	0	0	0	7	0	1	1	0	1	0	22	1	0	1	0	0	1	37	0	0	1	0	1	1	52
0	0	0	1	0	0	8	1	1	1	0	1	0	23	0	1	1	0	0	1	38	1	0	1	0	1	1	53
1	0	0	1	0	0	9	0	0	0	1	1	0	24	1	1	1	0	0	1	39	0	1	1	0	1	1	54
0	1	0	1	0	0	10	1	0	0	1	1	0	25	0	0	0	1	0	1	40	1	1	1	0	1	1	55
1	1	0	1	0	0	11	0	1	0	1	1	0	26	1	0	0	1	0	1	41	0	0	0	1	1	1	56
0	0	1	1	0	0	12	1	1	0	1	1	0	27	0	1	0	1	0	1	42							
1	0	1	1	0	0	13	0	0	1	1	1	0	28	1	1	0	1	0	1	43							
0	1	1	1	0	0	14	1	0	1	1	1	0	29	0	0	1	1	0	1	44							
1	1	1	1	0	0	15	0	1	1	1	1	0	30	1	0	1	1	0	1	45							

Ⓒ Data expansion C12, C13
These are set with the switches and used to expand commands.

Ⓓ Data judgment K (Refer to ※2.)
The last bit is for judgement of data transmission system. Date are transmitted as follows by using this bit.

※2: Data judgment
The data are not reversed in this case.

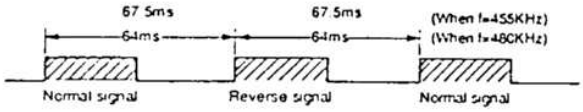
(a) Normal signals



(b) Reverse signals



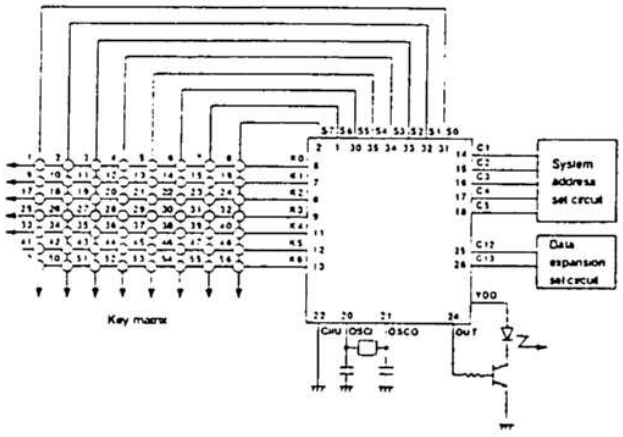
When the data judgment bit is "0," normal signals are transmitted. When it is "1," the reverse signals of C0 ~ C14 and K are transmitted.



As shown above, normal signals and reverse signals are repeated in series in a certain cycle. In the receiver side, judgment between normal and reverse signals is performed with the data judgement bit to form data properly.

Ⓔ Check bit C14
C14 is fixed to GND in the LSI and no pin is provided in the package.

(3) System configuration



When command [3] is sent, for example, press the key at the intersection between K0 and S2. The 15 bit data at that time is as follows:

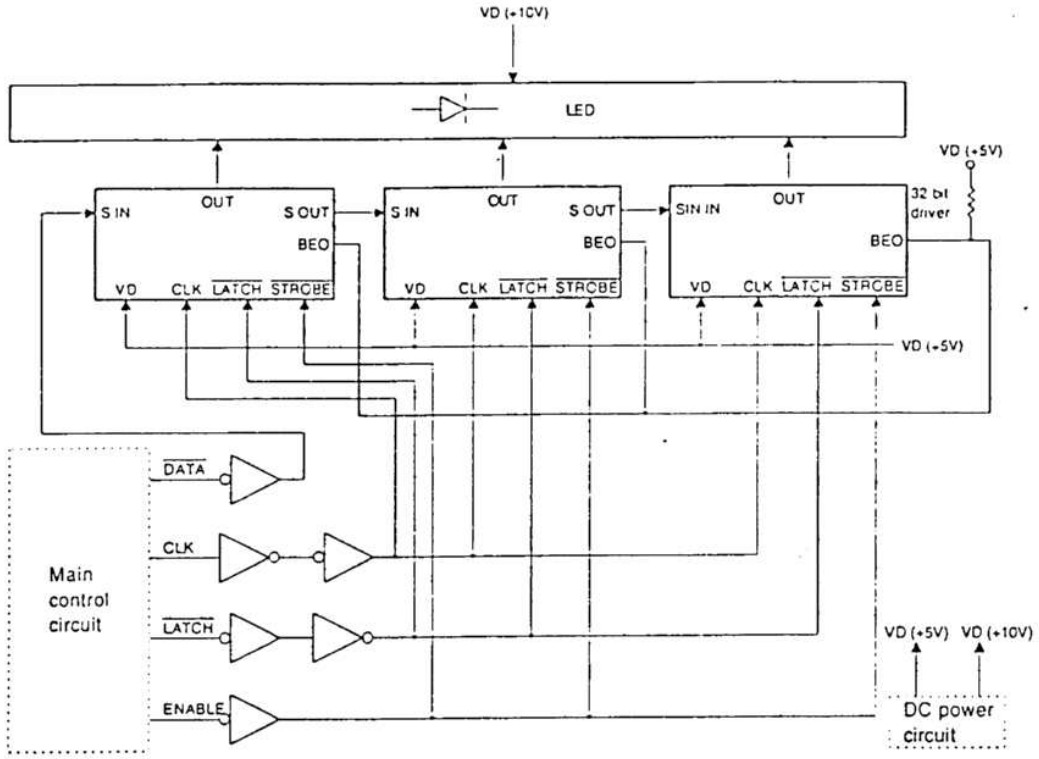
[3] 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0

System address bit Data bit

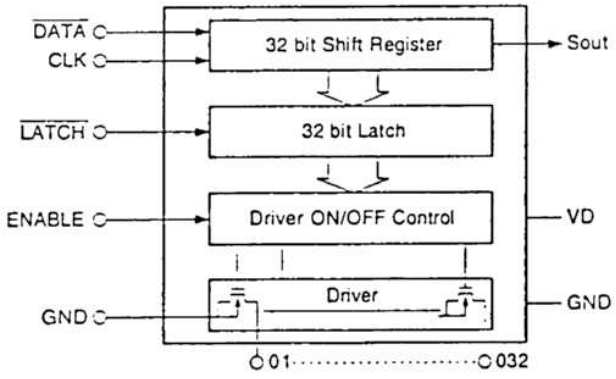
<Display circuit>

This circuit is controlled with the data signal and the control signal from the main control circuit.

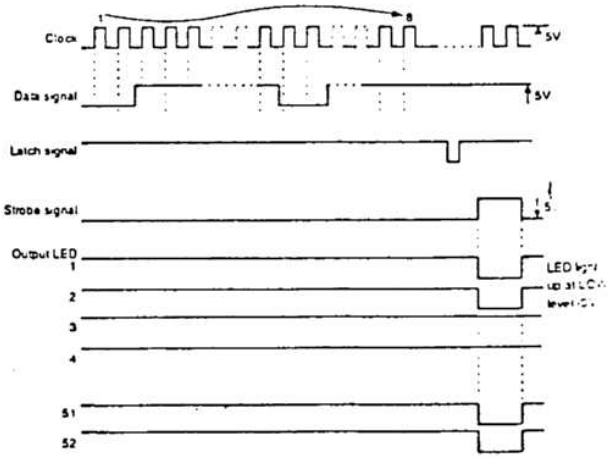
(1) Block diagram



32 bit driver block diagram



(2) Operational description

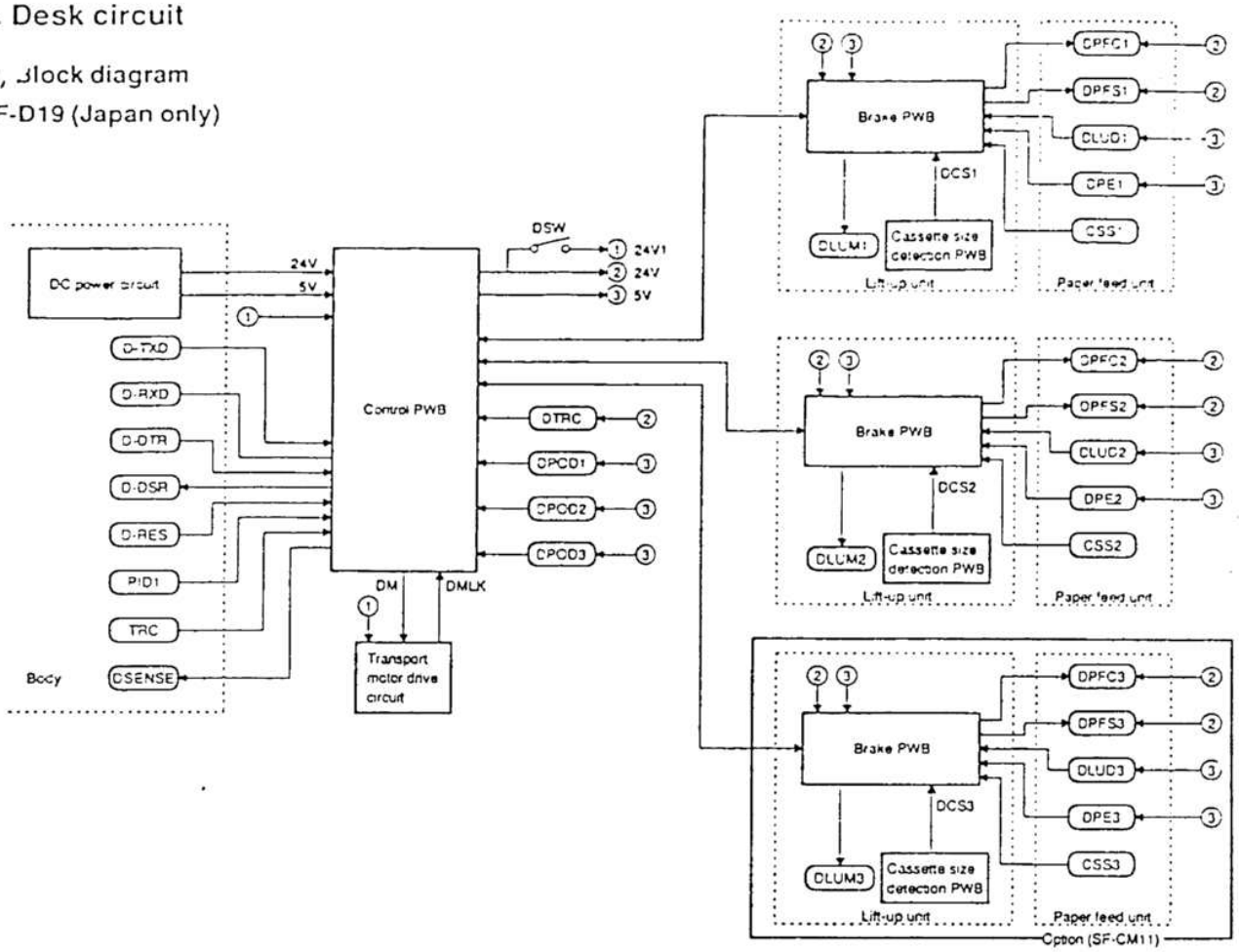


Data signals (8 bit) sent from the main control PWB are shifted at the rising timing of the clock and retained at the resign timing of the latch signal.
The retained data are outputted when STROBE signal becomes HIGH (5V), lighting the LED.

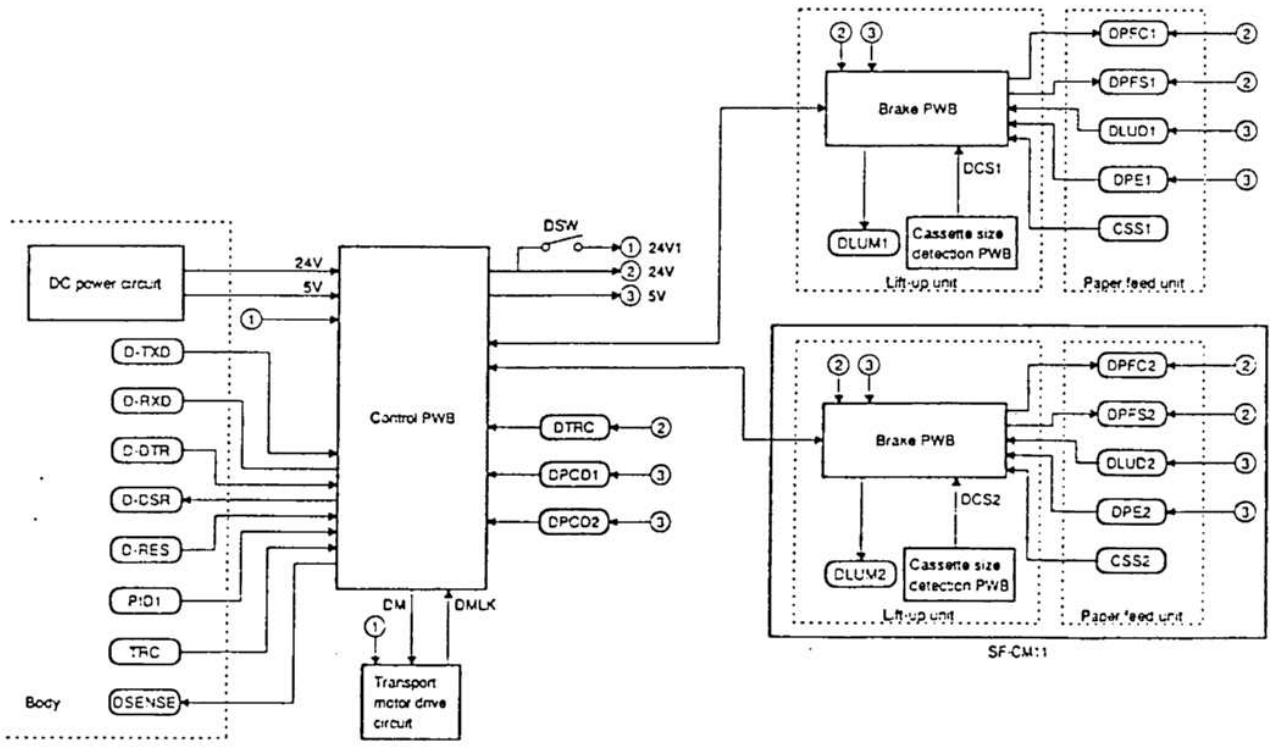
4. Desk circuit

(1) Block diagram

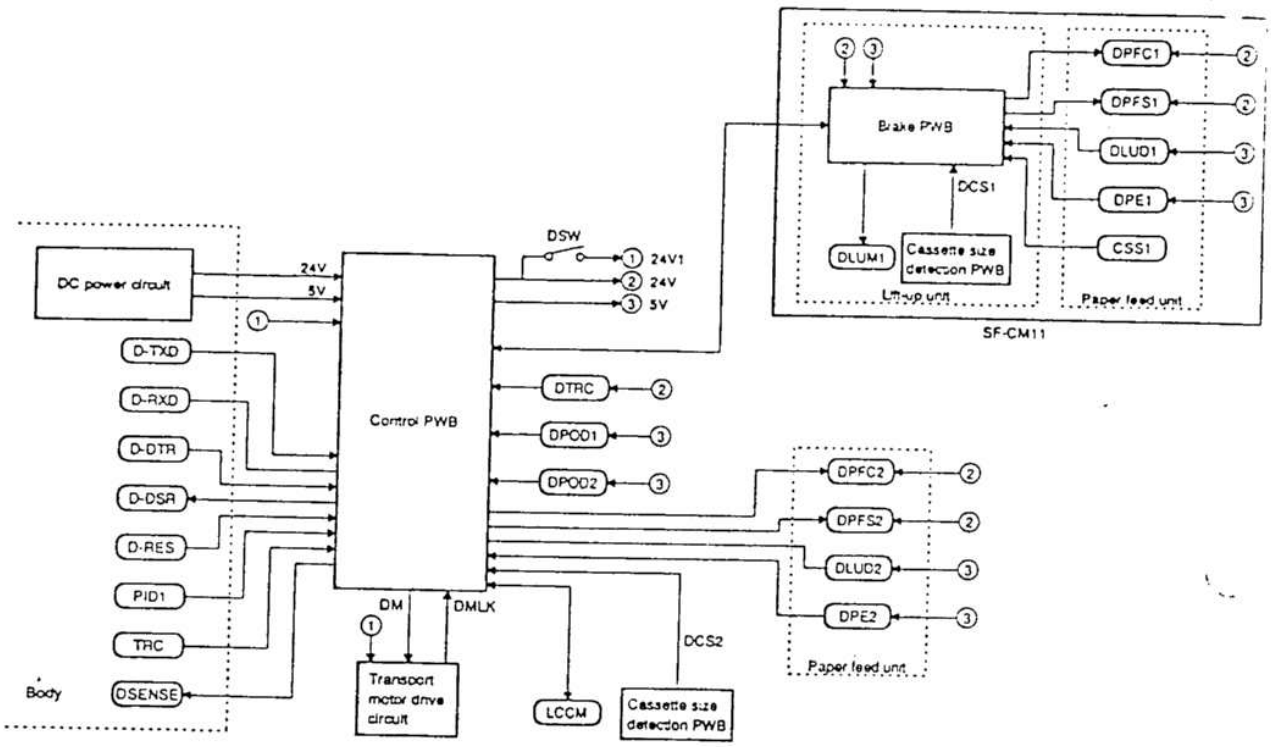
SF-D19 (Japan only)



SF-D20 (Overseas only)



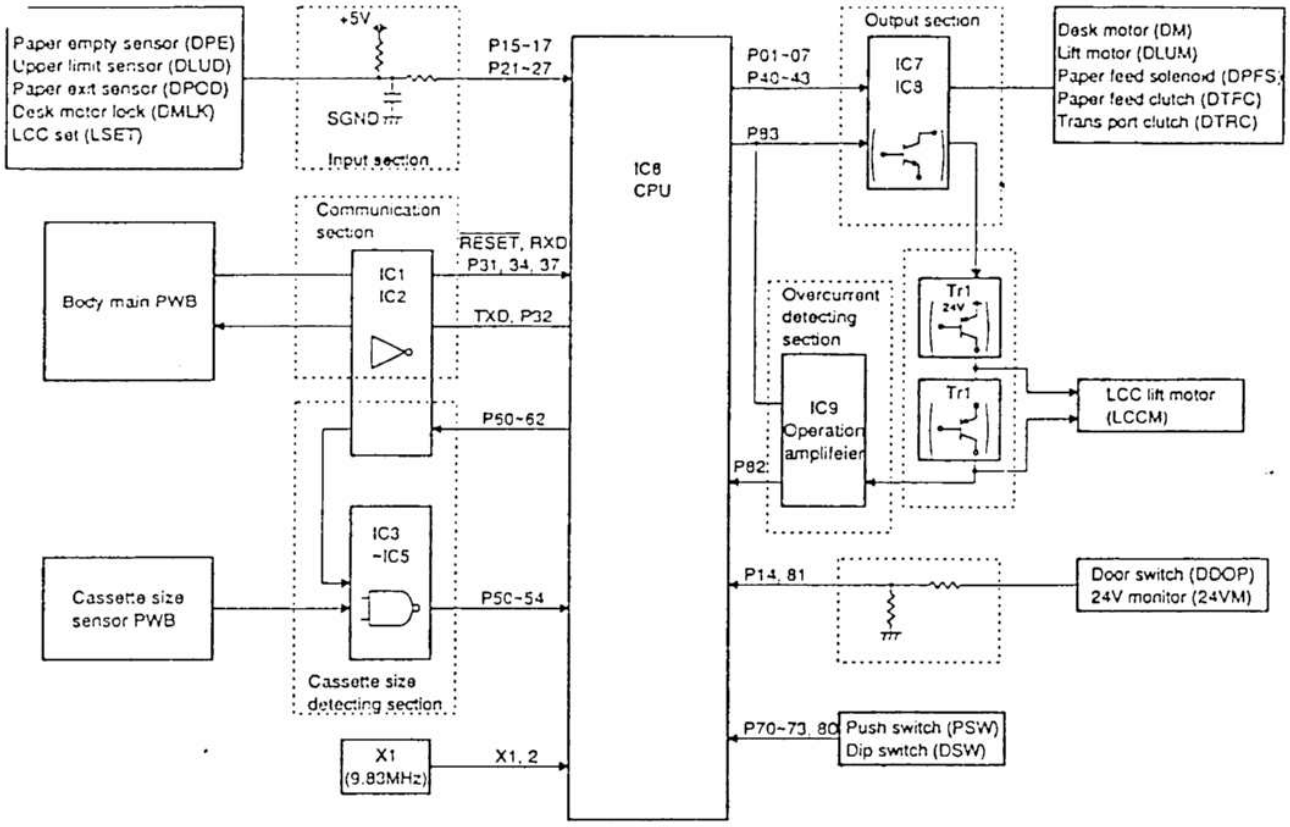
SF-D21 (Overseas only)



CSS1	Desk upper cassette size sensor 1
CSS2	Desk medium cassette size sensor 2
CSS3	Desk lower cassette size sensor 3
D-DSR	Data send ready
D-DTR	Data transmit ready from
D-RES	Desk CPU reset
D-RXD	Receive data to desk
D-TXD	Send data from desk
DLUD1	Desk upper lift up upper limit sensor 1
DLUD2	Desk medium lift up upper limit sensor 2
DLUD3	Desk lower lift up upper limit sensor 3
DLUM1	Desk upper lift up motor 1
DLUM2	Desk medium lift up motor 2
DLUM3	Desk lower lift up motor 3
DMLK	Desk motor lock
DM	Desk motor
DPE1	Desk upper paper presence/empty sensor 1

DPE2	Desk medium paper presence/empty sensor 2
DPE3	Desk lower paper presence/empty sensor 3
DPFC1	Desk upper paper feed clutch 1
DPFC2	Desk medium paper feed clutch 2
DPFC3	Desk lower paper feed clutch 3
DPFS1	Desk upper paper feed solenoid 1
DPFS2	Desk medium paper feed solenoid 2
DPFS3	Desk lower paper feed solenoid 3
DPOD1	Desk upper paper exit sensor 1
DPOD2	Desk medium paper exit sensor 2
DPOD3	Desk lower paper exit sensor 3
DESENSE	Not used.
DTRC	Desk transport roller clutch
LCCM	Large-scale cassette motor
PID1	Paper entry sensor
TRC	Transport roller clutch

(2) Circuit block diagram



Control PWB block diagram

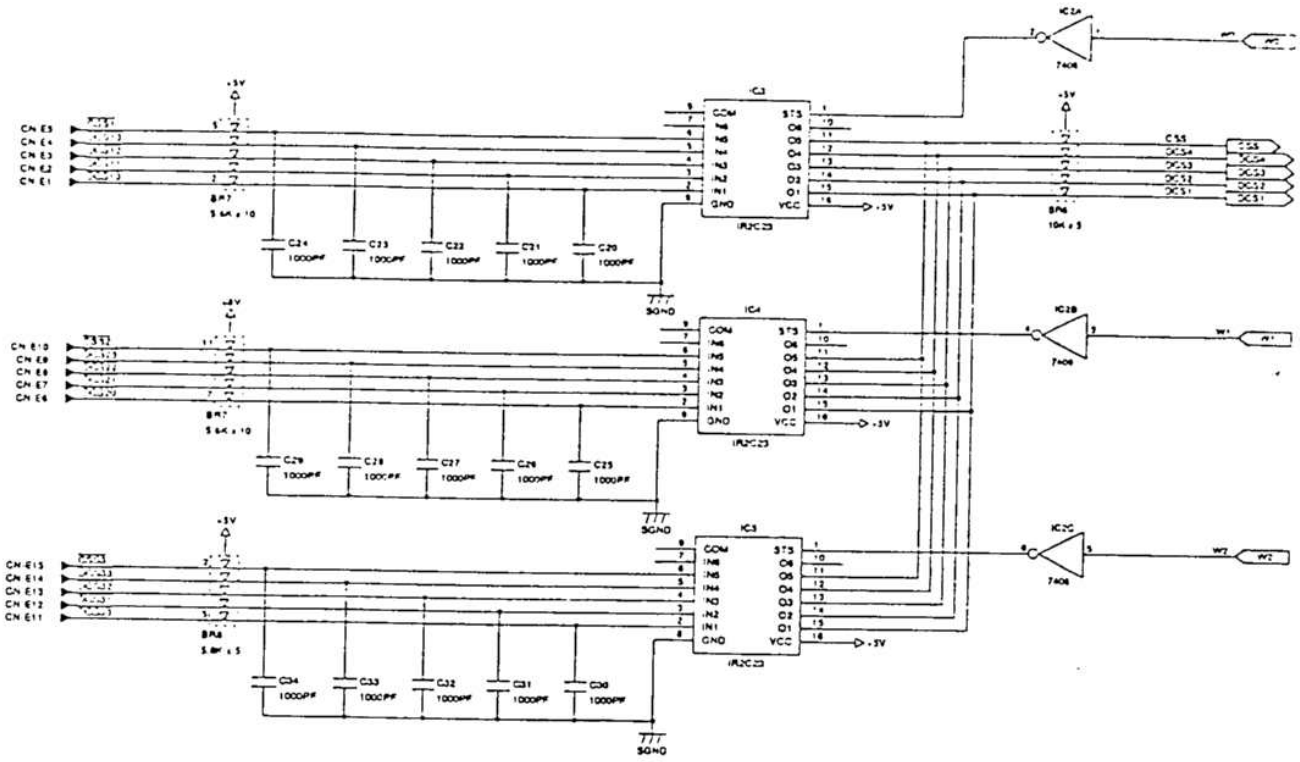
IC6 (CPU) pin signal

Pin No.	Pin name	IN/OUT	Signal name	Description
1	VREF		+5V	
2	AGND		SGND	
3~6	P50~53		$\overline{DCS1\sim4}$	Cassette size sense signal (Common to 1 - 3CS)
7	P54	IN	$\overline{CSS}$	Cassette presence signal (Common to 1 - 3CS). LOW (0V) when paper feed unit is attached.
	P55	IN		
9	P60	OUT	$\overline{W0}$	Data select signal. LOW (0V) when the upper cassette size data are read.
10	P61	OUT	$\overline{W1}$	Data select signal. LOW (0V) when the medium cassette size data are read.
11	P62	OUT	$\overline{W2}$	Data select signal. LOW (0V) when the lower cassette size data are read.
12	P63	–	–	Not used.
13~16	P70~73	IN	$\overline{DSW1\sim4}$	Dip switch. Used for selecting test mode.
17	P80	IN	$\overline{PSW}$	Push switch. Used for test mode operation.
18	P81	IN	$\overline{24VM}$	24V monitor signal. LOW (0V) when any abnormality in 24V is detected.
19	P82	IN	$\overline{OC}$	LCCM overcurrent signal. LOW (0V) when LCCM overcurrent is detected.
20	P83	OUT	LCCM	LCC lift motor control signal. Lifts up at HIGH (+5V).
21	$\overline{NMI}$	IN	$\overline{NMI}$	Pulled up to +5V.
22	$\overline{RESET}$		D-RES	Reset signal. Reset state at LOW (0V).
23	CLK	–	–	Not used.
24	P00	–	–	Not used.
25	P01	OUT	DM	Desk motor control signal. The desk motor rotates at HIGH (+5V).
3	P02	OUT	DLUM1	Upper lift motor control signal. The upper cassette is lifted up at HIGH (+5V).

Pin No.	Pin name	IN/OUT	Signal name	Description
27	P03	OUT	DLUM2	Medium lift motor control signal. The medium cassette is lifted up at HIGH (+5V).
28	P04	OUT	DLUM3	Lower lift motor control signal. The lower cassette is lifted up at HIGH (+5V).
29	P05	OUT	DPFS1	Upper paper feed solenoid control signal. Upper takeup roller falls at HIGH (+5V).
30	P06	OUT	DPFS2	Medium paper feed solenoid control signal. Medium takeup roller falls at HIGH (+5V).
31	P07	OUT	DPFS3	Lower paper feed solenoid control signal. Lower takeup roller falls at HIGH (+5V).
32	Vss		SGND	
33~34	X1~2		X1~2	Clock pulse (9.83MHz)
35~38	P10~13	IN	SGND	
39	P14	IN	$\overline{DDOP}$	Door open signal. LOW (0V) when the door is opened.
40	P15	IN	$\overline{LSET}$	LCC set signal. LOW (0V) when the LCC paper feed unit is installed.
41	P16	IN	DMLK	Desk motor lock signal. HIGH (+5V) when the desk motor lock signal is detected.
42	P17	IN	$\overline{DPE1}$	Upper cassette paper empty sensor signal. LOW (0V) when upper cassette paper empty.
43	P20	IN	$\overline{DPE2}$	Medium cassette paper empty sensor signal. LOW (0V) when medium cassette paper empty.
44	P21	IN	$\overline{DPE3}$	Lower cassette paper empty sensor signal. LOW (0V) when lower cassette paper empty.
45	P22	IN	DLUD1	Upper cassette upper limit sensor signal. HIGH (+5V) when the upper cassette reach, e upper limit.
46	P23	IN	DLUD2	Medium cassette upper limit sensor signal. HIGH (+5V) when the medium cassette reaches the upper limit.
47	P24	IN	DLUD3	Lower cassette upper limit sensor signal. HIGH (+5V) when the lower cassette reaches the upper limit.
48	P25	IN	DPOD1	Upper cassette paper out sensor signal. HIGH (+5V) when copy paper passes through.
49	P26	IN	DPOD2	Medium cassette paper out sensor signal. HIGH (+5V) when copy paper passes through.
50	P27	IN	DPOD3	Lower cassette paper out sensor signal. HIGH (+5V) when copy paper passes through.
51	P40	OUT	DTRC	Transport clutch control signal. HIGH (+5V) when the transport clutch is on.
52	P41	OUT	DPFC1	Upper cassette paper feed clutch control signal. HIGH (+5V) when the upper takeup roller rotates.
53	P42	OUT	DPFC2	Medium cassette paper feed clutch control signal. HIGH (+5V) when the medium takeup roller rotates.
54	P43	OUT	DPFC3	Lower cassette paper feed clutch control signal. HIGH (+5V) when the lower takeup roller rotates
55	$\overline{EA}$	IN	+5V	
56	RXD	IN	D-TXD	Communication data from the body. (Reception)
57	P31	IN	D-DTR	Send enable signal from the body. HIGH (+5V) when send enable.
58	P32	OUT	D-DSR	Send request signal from the body. HIGH (+5V) when send request.
59	TXD	OUT	D-RXD	Communication data to the body. (Send)
60	P34	IN	TRC	Body transport clutch signal. HIGH (+5V) when the body transport clutch is ON.
61~62	P35~36	–	–	Not used.
63	P37	IN	PID1	BOdy paper entry sensor signal. HIGH (+5V) when paper enters the body.
64	Vcc		+5V	

(3) Cassette size detecting section

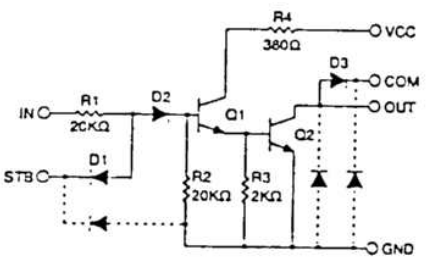
? data select signal of the desired cassette whose size data are red is driven LOW (0V). Then the other cassette size detecting signals are driven HIGH (+5V) and only the selected cassette size is read. The logic of the cassette size detecting signals are reversed and inputted to the CPU.

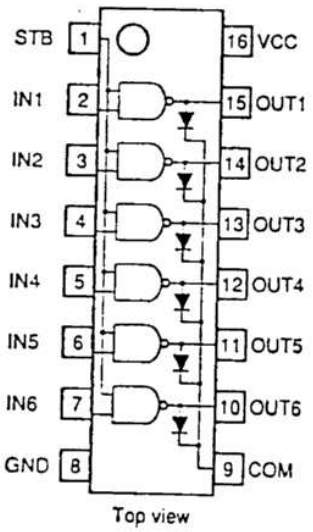


Circuit diagram

- IC3 - 5 (IR2C23)

Code	Pin name
STB	Strobe input pin
COM	COMMON pin
IN1~6	Input pin
OUT1~6	Output pin
V	Power pin
GND	GND pin

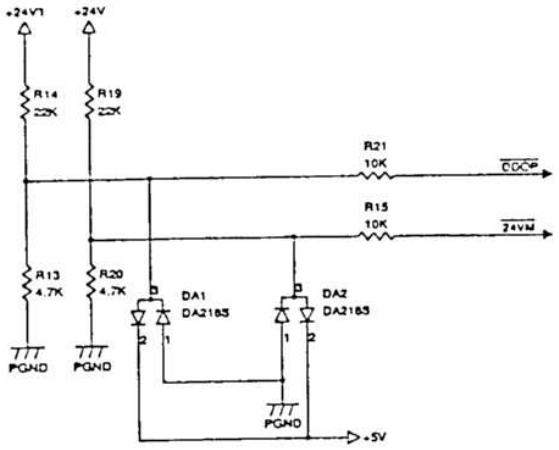




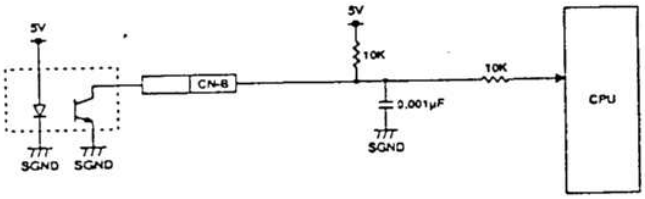
Top view

(4) 24V monitor and door open detecting section

This circuit monitors 24VM and DDOP to check conduction of +24V and +24V1. When the monitor signal is at HIGH (+5V), conduction is made.



- Input section

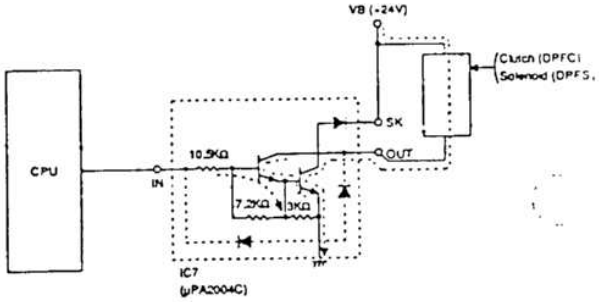


(5) Output section

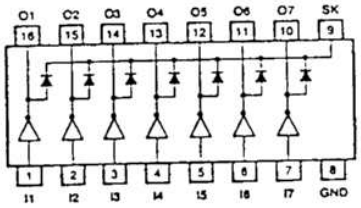
- Driver circuit

① General
The control signal of each load outputted from the CPU has no capacity to drive the load directly. The control signals, therefore are inputted to the driver IC to improve drive capacity then drive the loads (the solenoid, the magnetic clutch, etc.).
IC7 is the driver IC.

② Solenoid (DPFS), magnetic clutch (DPFC)
The drive circuit forms a Darlington circuit with two transistors to obtain a large drive current (load current) with a small input current (CPU output current). When the driver input voltage is high (+5V), the transistors conduct to flow a current in the arrow direction, operation the loads. When the driver is on, the driver output pin voltage is 0V.

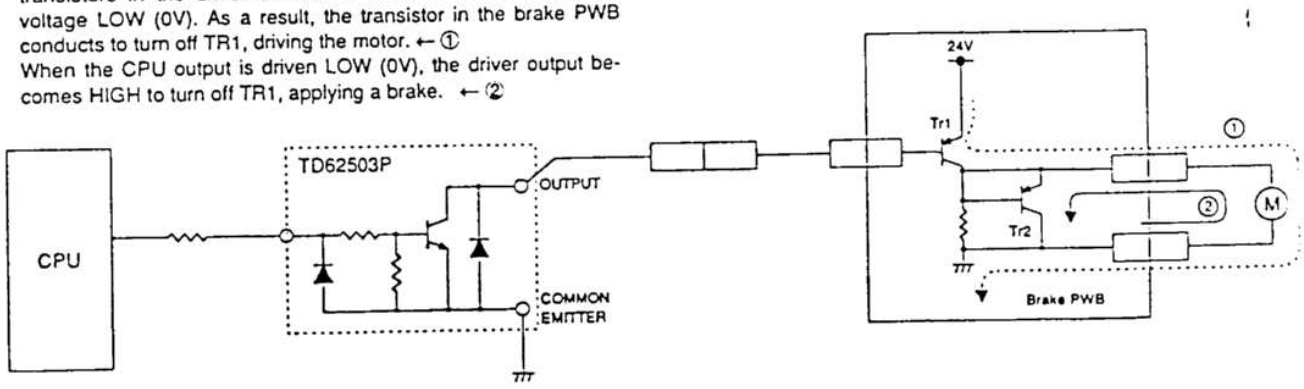


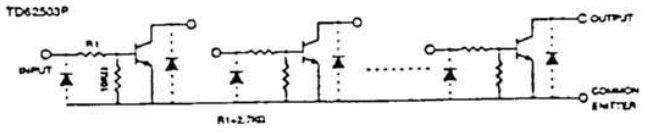
Pole connection (Top view)

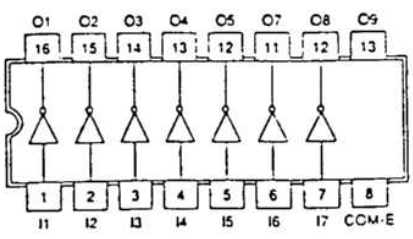


I : Input (Base)
O : Output (Collector)
GND (Common Emitter)

③ Desk motor (DM), lift motor (DLUM)
When the CPU output (driver input) voltage is HIGH (+5V), the transistors in the driver conduct to drive the driver output pin voltage LOW (0V). As a result, the transistor in the brake PWB conducts to turn off TR1, driving the motor. ← ①
When the CPU output is driven LOW (0V), the driver output becomes HIGH to turn off TR1, applying a brake. ← ②



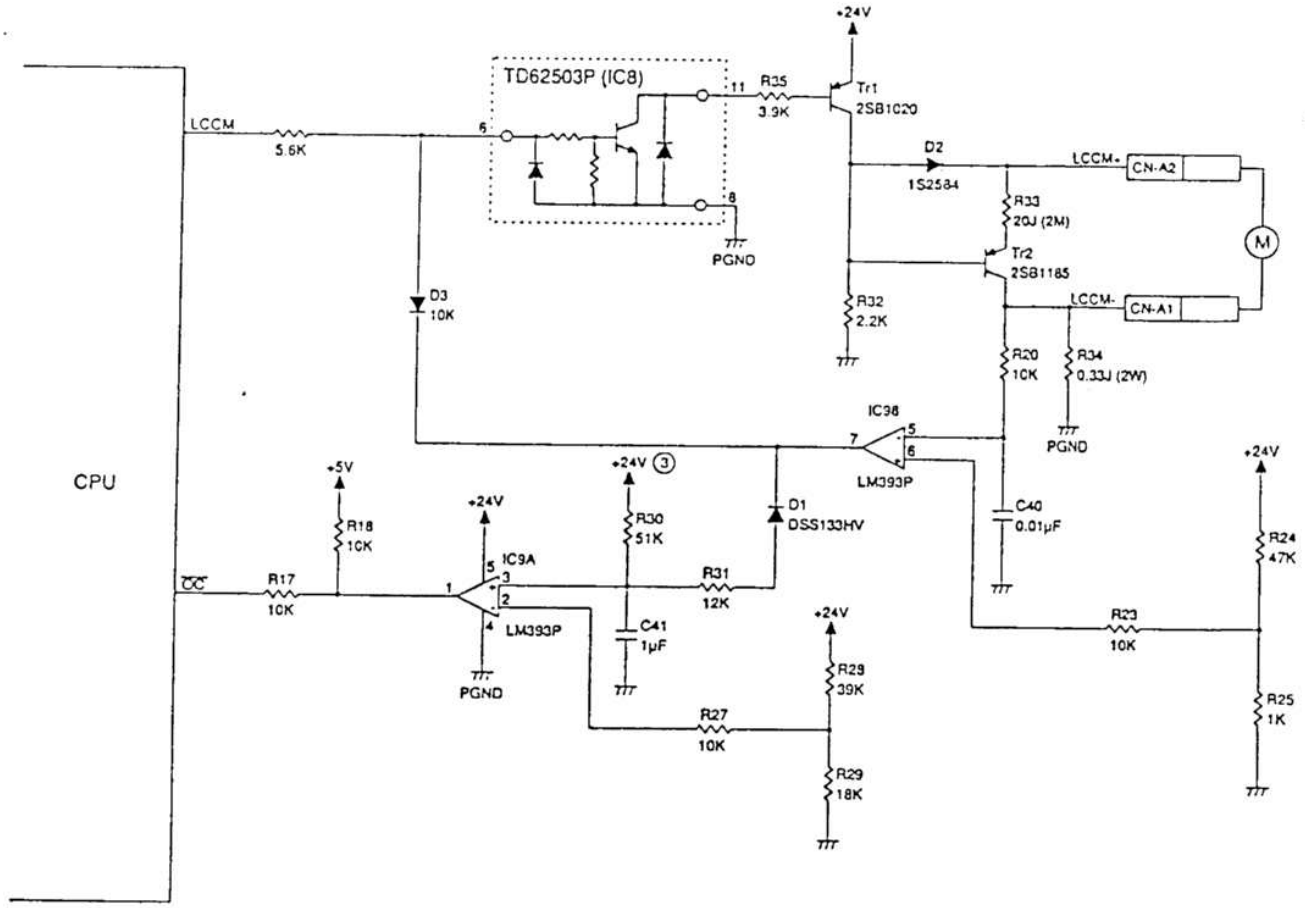




4 LCC lift motor (LCCM)
The operations are the same as (3). The brake circuit, however, is on the desk main PWB.

(6) Overcurrent detecting section

When the current flowing through the desk motor increases, the input voltage in the negative side of IC9B increases. When the input voltage exceeds the input voltage of the IC9B positive side, the IC9B output voltage is driven LOW (0V), pulling the motor signal, turning off TR1, and stopping the desk motor.
Since +24V of 3 is pulled at the same time, the IC9A positive side input voltage is driven LOW (0V) to be smaller than the IC9A negative side input voltage. As a result, the IC9A output voltage is driven LOW (0V). This drives the overcurrent detecting signal LOW (0V), detecting the desk motor overcurrent.



SF-2022
SF-2027

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SHARP CORPORATION
Printing & Reprographic Systems Gr
Quality & Reliability Control Center
Yamatokoriyama, Nara 639-11, Japan
1992 September Printed in Japan Ⓢ